Advanced High Frequency Soft-switching Converters for Automotive Applications

by

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ABSTRACT

Presently, hard-switching buck/boost converters are dominantly used for automotive applications. Automotive applications have stringent system requirements for dc-dc converters, such as wide input voltage range and limited EMI noise emission. High switching frequency of the dc-dc converters is much desired in automotive applications for avoiding AM band interference and for compact size. However, hard-switching buck converter is not suitable at high frequency operation because of its low efficiency. In addition, buck converter has high EMI noise due to its hard-switching. Therefore, soft-switching topologies are considered in this thesis work to improve the performance of the dc-dc converters.

Many soft-switching topologies are reviewed but none of them is well suited for the given automotive applications. Two soft-switching PWM converters are proposed in this work. For low power automotive POL applications, a new active-clamp buck converter is proposed. Comprehensive analysis of this converter is presented. A 2.2 MHz, 25 W active-clamp buck converter prototype with Si MOSFETs was designed and built. The experimental results verify the operation of the converter. For 12 V to 5 V conversion, the Si based prototype achieves a peak efficiency of 89.7%. To further improve the efficiency, GaN FETs are used and an optimized SR turn-off delay is employed. Then, a peak efficiency of 93.22% is achieved. The EMI test result shows significantly improved EMI performance of the proposed active-clamp buck converter. Last, large- and small-signal models of the proposed converter are derived and verified by simulation.

For automotive dual voltage system, a new bidirectional zero-voltage-transition (ZVT) converter with coupled-inductor is proposed in this work. With the coupled-inductor, the current to realize zero-voltage-switching (ZVS) of main switches is much reduced and the core loss is minimized. Detailed analysis and design considerations

for the proposed converter are presented. A 1 MHz, 250 W prototype is designed and constructed. The experimental results verify the operation. Peak efficiencies of 93.98% and 92.99% are achieved in buck mode and boost mode, respectively. Significant efficiency improvement is achieved from the efficiency comparison between the hard-switching buck converter and the proposed ZVT converter with coupled-inductor.

DEDICATED TO

My Parents: Yang Nan and Xia Li

My fiancée: Yue Wang

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Chapter 1

INTRODUCTION

1.1 Automotive Electrical System

In modern automobiles, electronic devices and electrical loads are ubiquitous. A reliable and high efficient power delivery system is essential to the operation of on-board electrical and electronic loads. This section covers the background on the automotive electrical systems, including current 14V PowerNet architecture and future 48V/14V dual voltage power architecture.

1.1.1 14V PowerNet Architecture

Currently, in most internal combustion engine (ICE) based passenger cars, 14V PowerNet architecture, as shown in Figure 1.1, is used for the automotive electrical system [1]. The electrical power is generated by the alternator, and the ac voltage of the alternator output is then rectified and connected to the 14-V dc bus. In addition, a 12-V lead-acid battery is connected to the dc bus as the backup power when the engine is off. During the ignition, the 12-V battery also provides the needed high current to the starter through the cranking system.

The electrical and electronic loads in vehicles are typically powered by point-of-load (POL) converters which are connected to the dc bus through fuses and relays protecting the wires against overheat. The POL converters convert the dc bus or battery voltage to different, well-regulated voltages like 1.8 V, 3.3 V or 5 V for the loads to use. Originally, most of these power converters are linear regulators which can regulate the output to the desired voltage while with low efficiency. With the

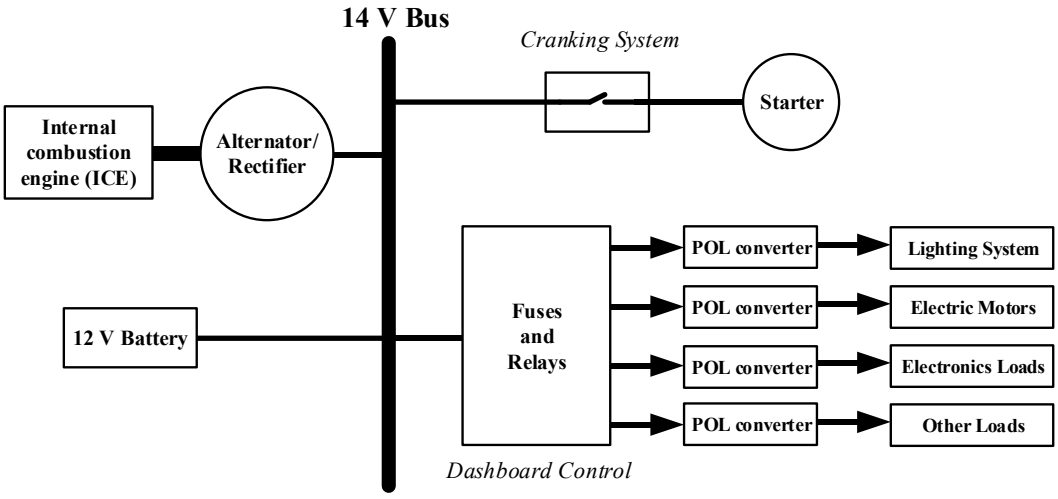

Figure 1.1: 14V PowerNet Architecture in Most Present Passenger Cars.

improvement of power electronics technology, most linear regulators in automobiles are now replaced by the high efficiency switching mode power supplies (SMPS). However, the research on further improving the efficiency of the SMPS is still desired, especially at increasing switching frequencies, to save fuel consumption and reduce CO^2 emissions. Development of high efficiency POL dc-dc converter for low power electronics loads is one of the research objectives in this thesis work.

1.1.2 48V/14V Dual Voltage Power Architecture

The 14V PowerNet architecture for passenger cars have been used for many years since around 1955. However, as ever increasing number of electrical and electronic equipments are being employed to support advanced functionalities, the 14V PowerNet will reach its limit. Nowadays, the total electronic and electrical loads on vehicles are around 2 kW and, in the future, the total electric power required by most internal combustion engine (ICE) based vehicles may exceed 5 kW [2]. With present 14V PowerNet, the high current level required by the high power loads will result in thicker and lossy wiring harnesses [3]. Therefore, 42V PowerNet was proposed in

late 1990s, by the researchers in MIT, to replace the 14V PowerNet [4]. However, the transferring from 14V PowerNet to 42V PowerNet was not successful in automotive industry due to many issues, and now this plan has been canceled.

Recently (in 2011), 48-V high voltage battery was introduced by German carmakers as a supplementary power supply, besides the conventional 12-V battery, for high power applications on vehicles, such as Electrical Power Steering (EPS), Electronic Braking Systems (EBS) and HVAC systems. With the 48-V battery, these loads can operate more efficiently and achieve better performance [5]. Moreover, wiring and component weight is reduced leading to reduced fuel consumption and CO^2 emissions. Meanwhile, 12-V battery is still kept for powering various low power loads, which are operated more efficiently with low dc bus voltage.

Since there are dual voltage systems on board, a bidirectional non-isolated dc-dc converter is required to connect the 48-V and 12-V batteries, as shown in Figure 1.2. In this dual voltage architecture, the alternator/rectifier as well as the starter are connected to the high voltage battery. Typically, the power rating of this bidirectional converter is up to 3 kW, according to alternator capacity. Another research objective in this thesis is to development high efficiency and compact bidirectional 48V/14V dc-dc converter for automotive dual voltage systems.

1.2 System Requirements for Automotive DC-DC Converters

Compared with many other applications, automotive application has some of the most challenging electrical and environment requirements for the design of dc-dc converters.

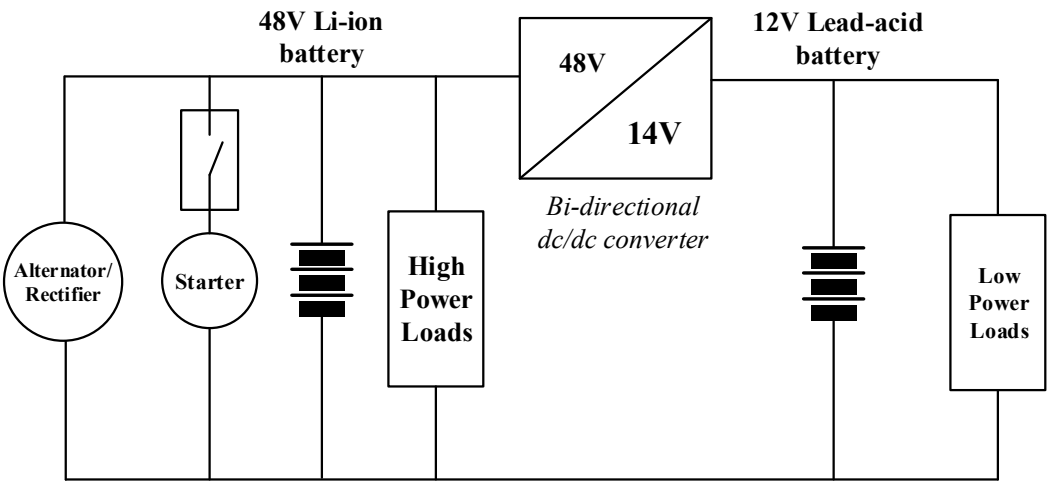

Figure 1.2: Automotive 48V/14V Dual Voltage Power Architecture.

1.2.1 Wide Input Voltage Range

The first design challenging for automotive dc-dc converters is the wide input voltage range. For the present 14V PowerNet architecture, the battery voltage ranges from 8 V to 16 V during most of the time [1]. This is the nominal operating input range for the downstream POL converters without function/performance restrictions. In the jump start situation, the dead battery may be hooked up to a 24-V automotive battery, like in a tow truck, through the jumper cable. Therefore, the vehicle with the dead battery is started with a 24-V battery and the power converters should work with the 24-V input voltage. Moreover, electrical and electromagnetic disturbances are frequently generated in an automotive environment. They will lead to voltage spike or voltage dip in the 14-V bus. One of the most well-known and destructive transients is the so-called load-dump, which refers to the disconnection of the battery from the alternator while the alternator is charging the battery [6]. This load dump may cause a voltage spike as high as 60 V. In most load dump situations, the 14-V bus voltage may reach 42 V. Thus, the POL converters connected to the 14-V bus should withstand an input voltage up to 42 V. Another well-known transient, on

the other side, is the voltage drop during the start of the engine (cranking) when the battery is delivering large current to the starter in a short time [7]. During the cranking, especially the cold cranking, the battery voltage may drop to 6.5 V or even 3.5 V (cold cranking) [8]. For some critical 5-V load that requires operation during cranking, a pre-boost converter may be employed to keep the input voltage of POL converters above 6 V or a higher voltage. In addition to the above two major disturbances, there are many other voltage transients presented at the 14-V bus or the battery, due to the turn-on and turn-off of the inductive loads. The test pulses of these transient disturbances are specified in SAE J1113/11 standard. For the design of the POL converters that connected to the 14-V bus, the immunity of the converters to these voltage transients should be concerned.

For 48V/14V dual voltage system, the wide input voltage range still exists. Although the voltage variation on 14-V bus is much reduced in dual voltage system, it could still range from 10 V to 16 V under different operating conditions. Regarding the 48-V bus, in most of the time, the bus voltage varies from 36 V to 52 V [5]. This is the nominal operating input range without function/performance restrictions for 48-V converters. During the large transients such as load dump and cold cranking, the 48-V bus voltage can reach 54 V and 24 V, respectively. Therefore, for the POL converters connected to 48-V or 14-V dc buses, and the bidirectional 48V/14V bus converter, the input voltage range is wide. This wide input voltage variation presents a big challenging for the converter design.

1.2.2 Strict EMI Limitation

Another challenging requirement is the strict CISPR-25 Standard for EMI performance of automotive dc-dc converters, as there are many on-board electronic devices susceptible to the EMI noise generated by the dc-dc converters. Usually the conducted

EMI emission problems could be mainly solved by the input EMI filters, besides the proper design and PCB layout of the dc-dc converter. However, the radiated EMI emission is much more complex and more difficult to solve, as the emission could not be attenuated directly by the EMI filters. The mitigation of the radiated emission is more like a system project as it involves the circuit design, components selection, PCB layout and shielding of the dc-dc converters.

It should be emphasized that the AM band, including the Medium wave (531 1611 kHz) and the Extended AM broadcast band (1610 1710 kHz), is the working frequency of many on-board RF receivers which are very susceptible to the noise over this frequency [9]. However, the automotive dc-dc converters with a switching frequency of hundreds of kHz is the major noise source within this frequency band. By the proper PCB layout, shielding and application of some other EMI mitigation techniques, such as spread spectrum, it is possible to reduce the radiated emission of the automotive dc-dc converters to the level below the limitation; but the best AM band EMI mitigation method is, applied at the design stage of the converter, pushing the switching frequency out of the AM band, either above 1.8 MHz or below 500 kHz. The switching frequency above 1.8 MHz is more desired since all the harmonics are outside the AM band. But this also presents another big challenging to the dc-dc converter design – high switching frequency.

Another thing should be noted is that, due to the strict EMI limitation, the PWM converter working at a constant switching frequency is much more desired compared to pulse frequency modulated converters, like resonant converters. This is because the EMI filter could be more effective and be designed more easily for PWM converters.

1.2.3 Compact Size and Light Weight

For most transportation applications, power converters' size and weight are always critical. In automobiles, the space for power converters is limited. With more and more electronic and electrical loads added in vehicles for advanced functionalities, increasing number of POL converters are required. The small size of converters is highly preferred. Weight of converters is also very critical for automobiles, since it affects the vehicle weight and hence the fuel consumption and acceleration performance of the vehicle. Therefore, compact size and light weight of the automotive dc-dc converters are desired. As well known, the most effective and direct way of shrinking the size and reducing the weight of dc-dc converters is increasing the switching frequency. Thus, for automotive dc-dc converters, high switching frequency is preferred.

1.2.4 Temperature Requirements

Another consideration of importance is the wide temperature range in automotive environment, which is critical to the proper operation of dc-dc converters. Depending on the location, the ambient temperature in a vehicle ranges from -40^{o} to more than 120^{o}. Therefore, for the dc-dc converters that may work under this temperature range, all the components in the converters should withstand the temperature stress. In addition, the high efficiency of the converter is desired for avoiding heating up components nearby the converter; and generally, the high efficiency is always desired for energy saving for all the power converters.

1.2.5 Feasibility of Interleaving

This is a requirement unique to automotive 48V/14V bidirectional converter. The power rating of this bus converter is typically 1 kW to 3 kW. If a single converter

is used to deliver the whole power, usually a large heatsink is required resulting in a bulky and heavy converter, which is not desired for automotive applications. Therefore, interleaving several converters is a preferred solution considering the good thermal management and flexibility for power scaling. If the power rating for each phase is low enough that the power loss could be dissipated without heatsink, the size and weight of the converter will be much reduced. Therefore, feasibility of interleaving is required for 48V/14V bidirectional converter.

1.3 Topology Review for Automotive DC-DC Converters

The design of the automotive dc-dc converters, including the topology selection, is a challenging task due to the aforementioned system and environment requirements. The major objective of this research is to develop suitable topologies for automotive low power POL converters and 48V/14V bidirectional converter at high switching frequency (MHz). At present, (synchronous) buck converter is dominantly used as the automotive POL converters and multiphase interleaved synchronous buck converter is widely accepted as the 48V/14V bidirectional converter for automotive dual voltage system. However, synchronous buck converter also presents some issues for automotive applications. In the following, synchronous buck converter is firstly reviewed from the efficiency and EMI point of view. Then, various non-isolated soft-switching techniques/converters are reviewed for two targeted applications, respectively.

1.3.1 Hard-switching Buck Converter

Synchronous buck converter, as shown in Figure 1.3, is widely employed in automotive and most other applications for voltage step-down owing to its simplicity, robustness, low cost and suitability for wide input voltage range. However, for the hard-switching (synchronous) buck converter, high switching frequency brings lots of

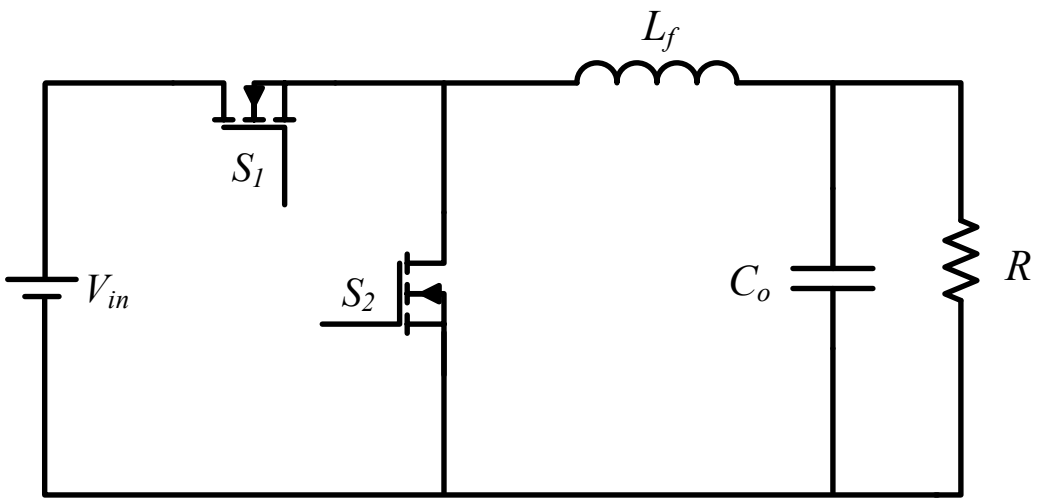

Figure 1.3: Diagram of A Conventional Buck Converter.

problems.

The first problem of buck converter is high frequency dependent losses in the circuit, including the switching device turn-on/off loss, body-diode reverse recovery loss, switching device output capacitance (C_{oss}) loss, gate drive loss, magnetic components core loss as well as the losses in parasitic inductance and capacitance. Among them, both switching turn-on/off loss and diode reverse recovery loss are partially determined by the device switching speed. Usually, in order to optimize the efficiency, the device switching speed (slew rate) is pushed high and hence the rise/fall time of switching is reduced. The switching loss is therefore reduced. But the rise/fall time cannot be arbitrarily reduced due to strict EMI requirements in automotive applications. Thus, with a reasonable slew rate of switching, it is difficult to achieve high efficiency for automotive buck converters at MHz switching frequency.

Another drawback of buck converter is its high EMI (especially radiated EMI) noise emission due to hard-switching. During the turn-off of the low side switch S_2, the reverse recovery of its body diode results in large current spike which further causes the voltage spike on S_2 through the resonance between stray inductance and

S_2 output capacitance. This process generates high EMI noise. Another EMI noise source is S_1 output capacitance discharging during the turn-on of S_1. The large EMI noise emission also poses a big challenging for the design. Usually the slew rate of switching is limited to obtain a better EMI performance at the cost of high switching losses. Sometimes, the spread spectrum technique is used to dither the switching frequency and hence spread the noise spectrum. It helps the converter to pass the EMI standard regulation although the total noise energy is not reduced. Shielding is another way to block the noise but at high cost.

From above discussion, it could be seen that buck converter, although being widely used in the industry because of its simple circuitry and low cost, might not be the most suitable topology for the automotive dc-dc converters. It is not efficient under high frequency operation and it does not have a desired EMI performance as well. To resolve the two above issues with buck converter, a soft-switching converter with fixed switching frequency is considered a good replacement, due to its low EMI noise emission and potential to achieve high efficiency at MHz switching frequency.

1.3.2 Soft-switching Converters

In this section, the concept of soft-switching is firstly introduced, followed by a brief review of various kinds of soft-switching converters. Then, detailed topology review for low power automotive POL converters and 48V/14V bidirectional converter are presented.

The soft-switching is a concept on the contrary to the hard-switching. Figure 1.4 shows the switching waveforms in hard-switching and soft-switching converters. In hard-switching converters, there is an overlap between $v_{sw}(t)$ and $i_{sw}(t)$ during switching. This overlap indicates the energy loss in the switch. While in the soft-switching converters, this $v_{sw}(t) - i_{sw}(t)$ overlap is eliminated by outside circuit of

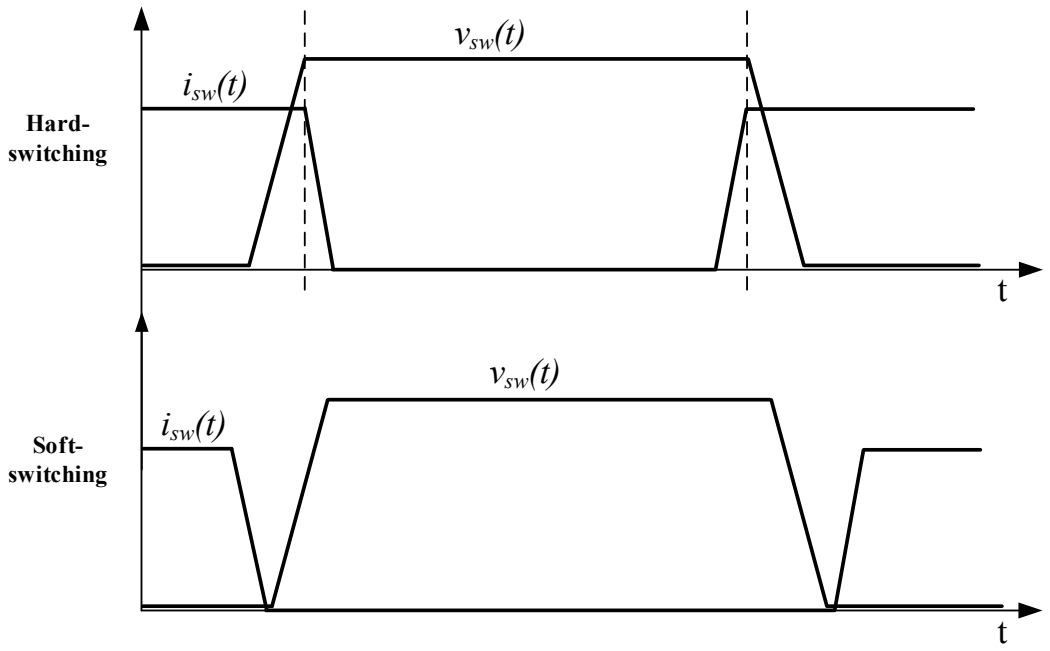

Figure 1.4: Switching Waveforms of Hard-switching and Soft-switching Converters.

the device.

Numerous soft-switching topologies have been proposed since the very first introduction of soft-switching concept in [10]. Basically, there are two kinds of soft-switching mechanisms: 1) zero-voltage-switching (ZVS) and 2) zero-current-switching (ZCS). In ZVS circuit, the switch voltage is brought to zero before gate voltage is applied. This turn-on transition is ideally loss-less. During the turn-off, capacitor paralleled with device acts as a loss-less snubber and the $v_{sw}(t) - i_{sw}(t)$ overlap is hence small. While in ZCS circuit, the switch current is brought to zero before gate voltage is removed. Ideally, this turn-off transition is loss-less. For the turn-on transition, the inductor in series with the switch acts a loss-less snubber leading to a small $v_{sw}(t) - i_{sw}(t)$ overlap. It should be noticed that, in ZCS circuit, the energy stored in junction capacitance of the switch is dissipated during turn-on transition. Generally, ZVS is more desired for high frequency converters with MOSFETs since it removes all major losses during switching. ZCS is more suited for converters with IGBTs due

to tail-current at turn-off. Therefore, in the following review, ZVS circuit is more focused.

The soft-switching converters could be classified into several types: 1) resonant converters; 2) quasi-resonant converters and 3) resonant transition converters. The resonant converter includes series resonant converter, parallel resonant converter, etc.. Usually, the output of resonant converter is regulated through frequency modulation. The quasi-resonant converters [11], constant-frequency multi-resonant converter [12, 13] are the converters that are based on quasi-resonant switches. The major issues of quasi-resonant converter is high voltage stress for switches. Due to the resonant approach, the peak voltage across the switch is more than twice the input voltage, which necessitates the use of switches with much higher voltage rating and hence on-resistance. The multi-resonant converter requires lower voltage rating (still higher than input voltage) compared to quasi-resonant converter, but it has much larger current stress in switches which increases the conduction loss significantly. Another issue of resonant and quasi-resonant is the difficulty of employing PWM control scheme. Although constant-frequency control could be used, it will increase the voltage/current stresses of the switch [14]. Unlike first two types of soft-switching converter, resonant transition converters, including zero-voltage-transition converters [15–18] and zero-current-transition converters [19], have the $L-C$ resonance happens only during the switch transition and PWM control scheme could be used. Typically, the voltage stress in this type of soft-switching converters is less than that in a counterpart resonant converters.

For the given automotive applications, since fixed frequency control is much desired, resonant transition converters, specifically the zero-voltage-transition (ZVT) converters are reviewed in more detail.

1.3.3 Topology Review for Low Power Automotive POL converters

A very simple ZVT converter is the quasi-square-wave (QSW) buck converter [16]. The switches in QSW converter have the voltage rating same as the input voltage. However, this converter has large current ripple on the inductor. Moreover, the current ripple increases significantly when input voltage reduces unless the undesired variable switching frequency is employed. Thus, it is not suitable for automotive applications that with wide input voltage range.

The ZVT PWM converter in [15] employs an auxiliary cell consisting of a switch, a diode and a small inductor to achieve ZVS of main switches. There are many ZVT converters consisting a similar auxiliary cell and some of them were evaluated in [20]. Generally, for automotive low power applications, this kind of ZVS converter has relatively large conduction loss in the auxiliary cell.

Passive lossless snubber method [21–23] also helps to achieve ZVS but is less efficient in low power operations [24]. Generally, passive snubber method leads to high voltage or current stress on switches and is not suitable for low power and wide input voltage range applications.

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Besides the aforementioned methods, active-clamp is another technique to realize ZVS and high efficiency operations in isolated flyback or forward converters [25–31]. It can also be used in non-isolated dc-dc converters, similar to the switched snubber concept proposed in [32]. References [33–35] proposed several families of active-clamp converters for relatively high power applications; however, the active-clamp buck con-

verter discussed in [34,36] has unclamped voltage spike on output rectifier. Thus, high voltage rating device is needed for the output rectifier and the efficiency is impacted. The improved active-clamp buck converter discussed in [35, 37] can prevent the voltage spike by using a clamp diode. However, the energy is not saved but dissipated in the clamp diode as conduction loss and it does not help improve the overall efficiency. References [38–41] proposed several coupled-inductor based active-clamp buck or boost converters. The coupled-inductor was introduced to increase the conversion gain and extend the duty cycle, and the active-clamp circuit is employed to recycle the energy stored in the leakage of the coupled-inductor. However, these are not suitable for the targeted applications of this paper, because the duty cycle range is wide under the wide input voltage. With the coupled-inductor, the duty cycle will be close to 100% under the lowest input voltage. This will result in a very large voltage across the clamp capacitor. Furthermore, the coupled-inductor based active-clamp buck converters discussed in above references still have no voltage spike clamping ([38, 39]) or lossy voltage spike clamping ([40, 41]) for the synchronous output rectifier, affecting the overall efficiency. Another issue of the coupled-inductor is the high cost. Proposed in [42] is a non-synchronous active-clamp boost converter demonstrating high efficiency for power-factor-correction (PFC) applications. Generally, one major issue of active-clamp converter is that it is not well suited for high current applications, since the resonant current ripple would be twice the filter inductor current, increasing the current ripple and hence conduction loss in resonant inductor and the synchronous switch. However, for the relatively low current applications, active-clamp based topologies are a good choice at MHz switching frequency.

1.3.4 Topology Review for 48V/14V dual voltage system

For this high current and high power application, the ZVT converter employing an auxiliary cell is more suitable. However, the basic ZVT buck converter proposed in [15] also has some issues. The auxiliary switch in [15] suffers hard-switching turn-off. In addition, the ZVT auxiliary cell locates at high voltage side and consequently, the voltage stress of auxiliary switches is at the voltage level of high voltage side. In [43, 44], coupled-inductor is employed to achieve ZCS turn-off of the auxiliary switches. Nevertheless, the voltage stress of the auxiliary switches is further increased by employing the coupled-inductor. In addition, the converters proposed in [44] still require a resonant inductor besides the coupled-inductor.

The ZVT auxiliary cell, instead of being located at the high voltage side, could also be placed at low voltage side [45–47]. Therefore, the voltage stresses of two auxiliary switches (both auxiliary switches are active-switches for bidirectional application) are reduced to the low side voltage and the difference voltage between high side and low side, respectively. Moreover, ZCS is achieved for auxiliary switches at both turn-on and turn-off instants. This type of ZVT converter also shows better efficiency and EMI performance among several ZVT converters [20]. However, for high current applications, the current magnitude and duration in the auxiliary cell is large, resulting in a large conduction loss in the cell. Especially, at higher frequency operation this conduction loss is even worse since the total conduction time of the auxiliary cell is fixed while the switching period is reduced.

1.3.5 Objective, Contributions and Organization of the Thesis

The objective of this work is to develop suitable topologies, for automotive low power POL converters and 48V/14V bus converter, which can achieve high efficiency

and generate low EMI noise at MHz switching frequency.

In Chapter 2, a new active-clamp buck converter with synchronous rectification (SR) is proposed for 2.2 MHz, low power (25 W) automotive POL applications. With the added active-clamp circuit, this converter has the advantages of 1) ZVS for all three switches; 2) soft turn-off of SR with much lower di/dt rate; 3) clamped voltage stress for all switches; and 4) high efficiency and low EMI operation due to the soft-switching. In addition, the added energy recovery clamp diode can clamp the voltage spike on SR and, at the same time, recover partial spike energy to the clamp capacitor. The operating principle of the converter, detailed analysis and design according to the given specifications are presented. The experimental results from a 2.2 MHz, 5V/5A prototype converter with Si MOSFETs demonstrates the superior performance of the proposed active-clamp buck topology. Then, GaN devices are employed to further improve the efficiency. Last, the modeling of the proposed active-clamp buck converter is investigated. Large-signal and small-signal models are derived with the verification in PLECS and Simplis, respectively.

In Chapter 3, for automotive 48V/14V dual voltage system, a new bidirectional ZVT PWM converter with coupled-inductor is proposed. With the combination of ZVT circuit and the coupled-inductor, this topology features 1) ZVS for main switches and ZCS for auxiliary switches; 2) reduced current and hence conduction loss in the auxiliary cell; 3) high efficiency and low EMI noise operation; 4) compact size of the converter and 5)flexibility for interleaving and power scaling. The detailed analysis, circuit design and implementation are presented. A 1 MHz, 250 W prototype was constructed and tested. The experimental results verify the converter operation and show the good efficiency performance.

Chapter 4 covers the conclusion of this thesis work.

Chapter 2

ACTIVE-CLAMP BUCK CONVERTER FOR AUTOMOTIVE LOW POWER POL CONVERTERS

2.1 Introduction

In this chapter, a new active-clamp buck converter is proposed for low power automotive POL applications. The circuit diagram of the proposed active-clamp buck converter is shown in Figure 2.1. An auxiliary network, consisting of auxiliary switch S_2, resonant inductor L_r, clamp capacitor C_{clamp}, and clamp diode D_{clamp}, is incorporated into the synchronous buck converter. C_{r1} and C_{r2} are the combinations of extra paralleled resonant capacitors and the output capacitance of MOSFET S_1 and S_2, respectively. C_j and C_{oss} are the output capacitances of the clamp diode D_{clamp} and the synchronous rectifier SR, respectively. With the added auxiliary network, all three MOSFETs can achieve ZVS operation. The ZVS of S_1 is realized by the energy stored in L_r through the resonance between C_{r1}, C_{r2} and L_r, while the energy for achieving ZVS of S_2 and SR comes from the large filter inductor L_f, similar to the ZVS mechanism of the synchronous rectifier in synchronous buck converter. The resonant inductor L_r inserted between S_1 and SR helps to realize the soft turn-off of SR, further improving the conversion efficiency and EMI performance. The clamp diode D_{clamp} is placed between the drain nodes of S_2 and SR, in order to clamp the SR voltage spike and recover partial energy in the resonant inductor when SR turns off.

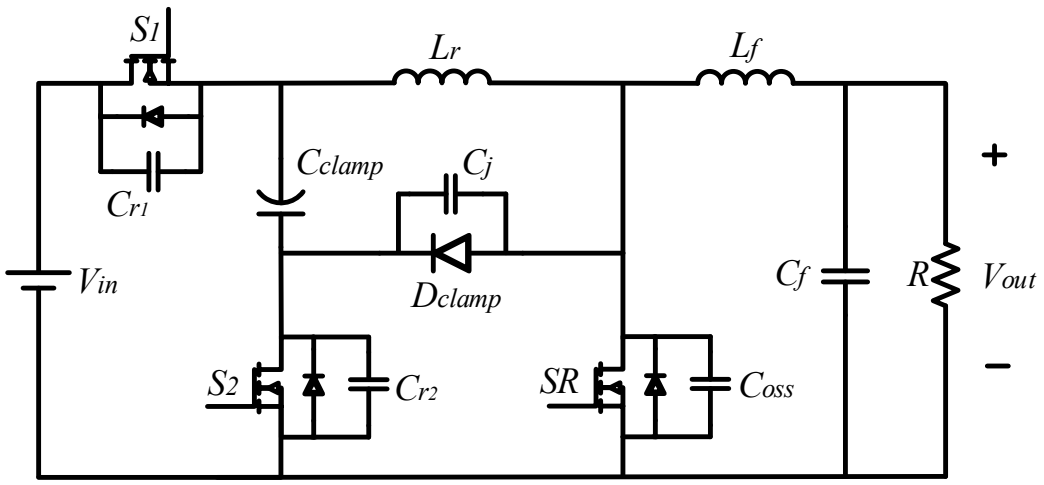


Figure 2.1: Circuit Diagram of the Proposed Active-clamp Buck Converter.

2.2 Operating Principle Analysis

To simplify the analysis of operating principle, the filter inductor is assumed sufficiently large so that the output filter (L_f and C_f) and load together could be considered as a constant current source (sink) I_{out}. Similarly, it is assumed that C_{clamp} is large enough and hence the voltage ripple is negligible; thus, C_{clamp} is represented by a constant voltage source V_{clamp}. The simplified circuit for operation analysis is shown in Figure 2.2. The arrows in Figure 2.2 indicate the reference direction for currents in the analysis. In addition, the MOSFET on-resistance, and the forward voltage drop of the MOSFET body-diodes and the clamp diode are ignored in analysis. However, all the parasitic capacitances of the switches are included in analysis. It also should be noted that C_{r1} and C_{r2} are assumed equal to C_r because S_1 and S_2 employ the same type of MOSFET. Figure 2.3 shows the key operating waveforms of the proposed active-clamp buck converter during one switching cycle and Figure 2.4 shows the topological states in each mode. The operating principle is described as below.

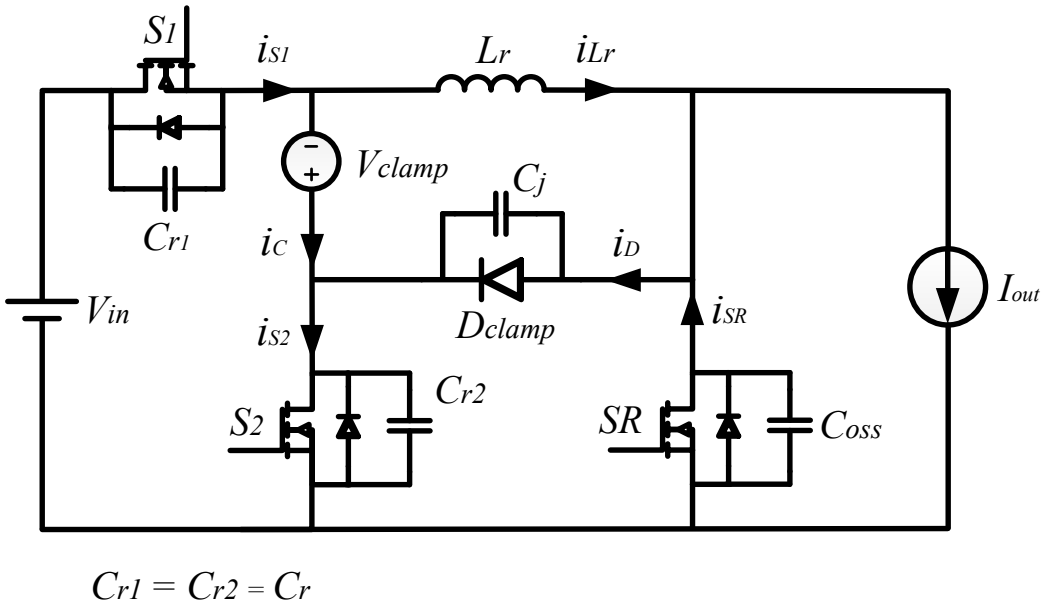


Figure 2.2: Simplified Circuit Diagram for Operating Principle Analysis.

Mode 0 $(t_{10} - t_0)$

Prior to t_0, main switch S_1 is on and the entire load current I_{out} flows through S_1 and L_r. At the same time, S_2 is off blocking a clamped voltage of V_s that amounts to $V_{in} + V_{clamp}$, SR is off blocking input voltage V_{in}, and D_{clamp} is off blocking a voltage of V_{clamp}.

Mode 1 $(t_0 - t_1)$

At t_0, the main switch S_1 is turned off and the load current I_{out} is divided into three parts, namely i_{s1}, i_{s2}, i_{SR}, charging the resonant capacitor of S_1 and discharging the other capacitors, as shown in Figure 2.4. The difference between the output current I_{out} and the resonant inductor current i_{Lr}, denoted as i_{diff}, is the current reduction in L_r during this mode and is expressed as

$$i_{diff} = \int \frac{V_{clamp} - v_{Dclamp}(t)}{L_r} \mathrm{dt} \tag{2.1}$$

where $v_{Dclamp}(t)$ is the instantaneous voltage across D_{Clamp}.

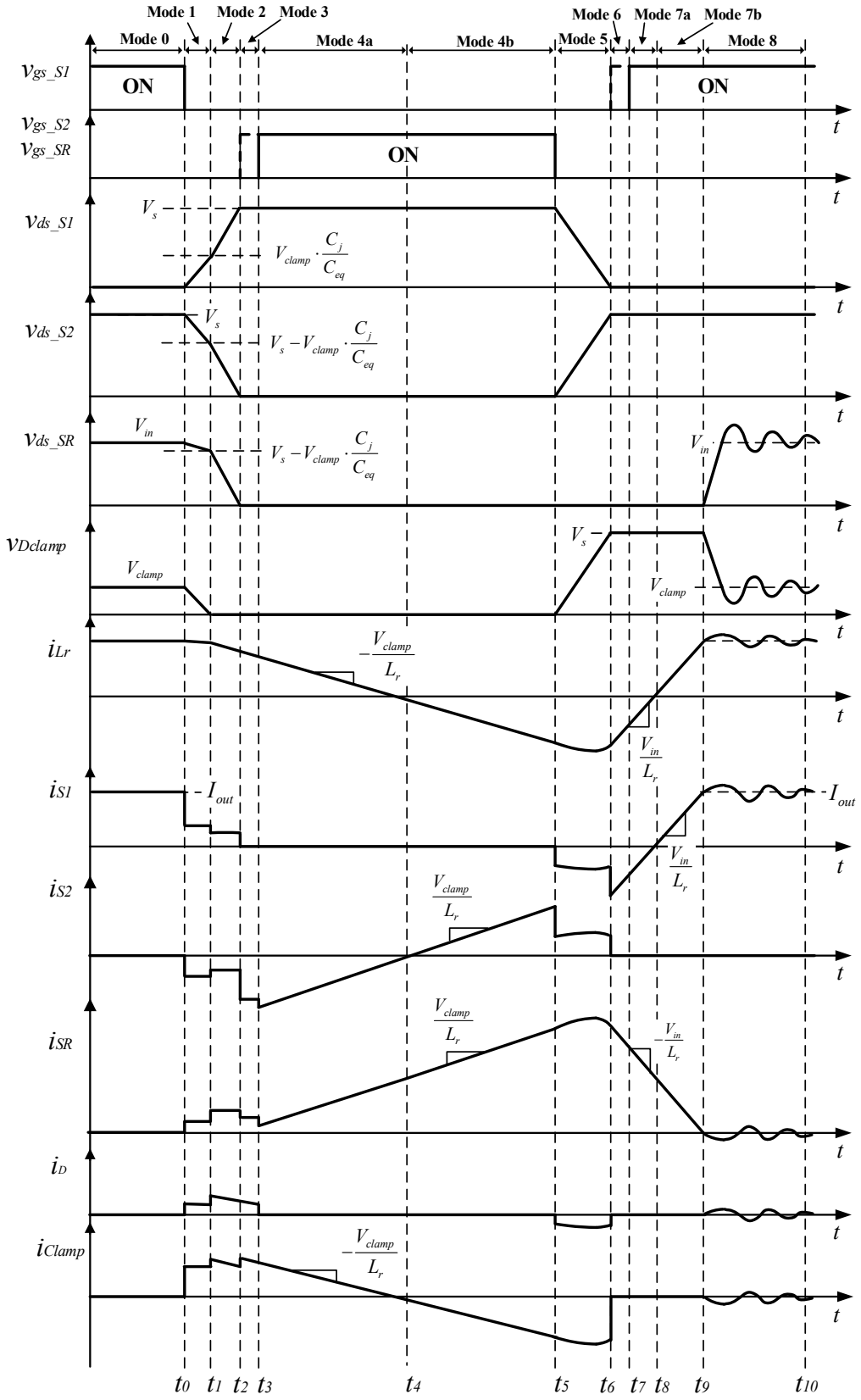


Figure 2.3: Key Operating Waveforms in a Switching Cycle (Corresponds to Assigned Current Direction in Figure. 2.2).

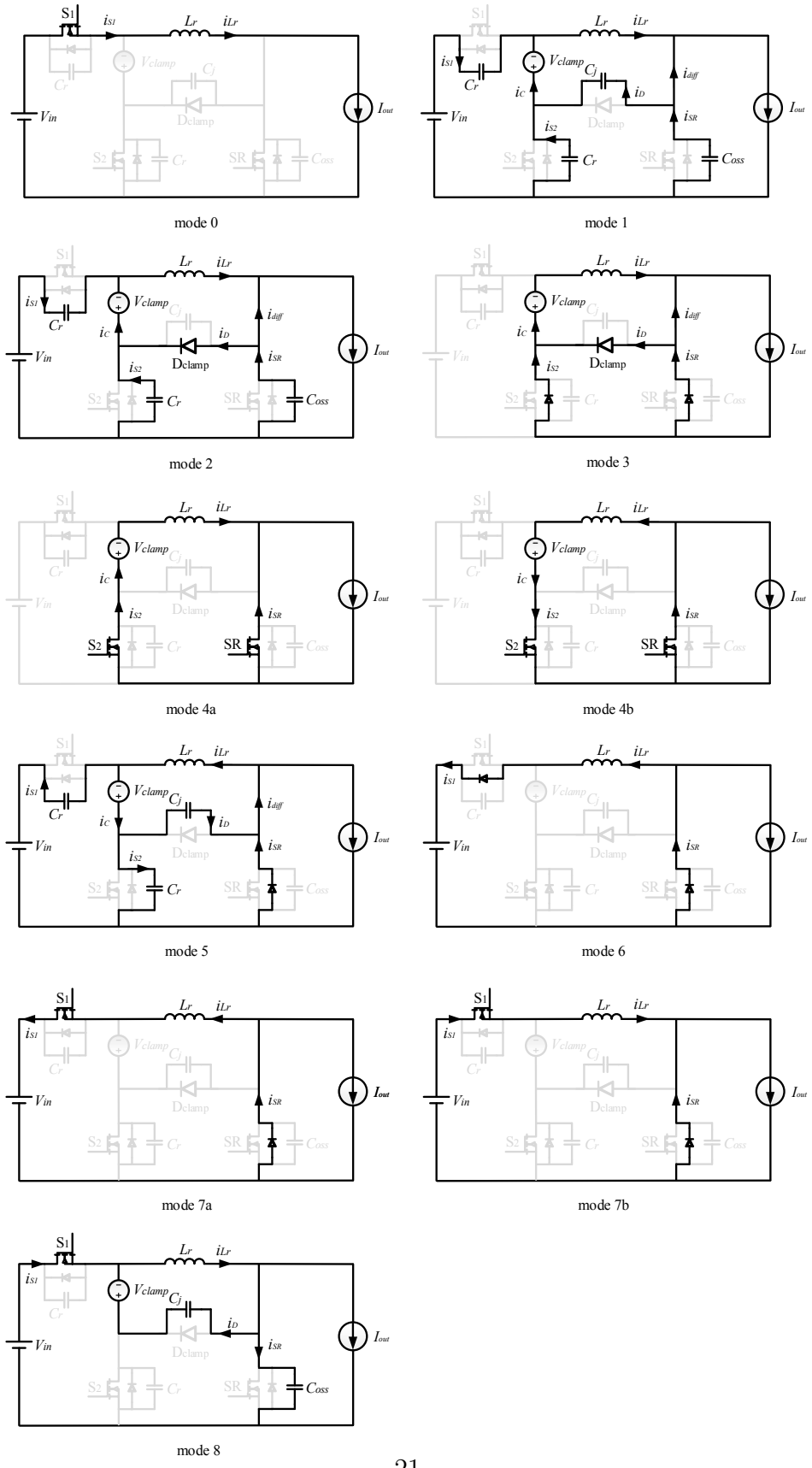


Figure 2.4: Topological States in Each Mode (the Arrows Indicate the Actual Direction of Current).

Since the V_{clamp} is not large by proper design and the time interval in this mode is very short, then the i_{diff} is almost zero during this mode and consequently, i_{Lr} equals to I_{out}. The D_{Clamp} discharge current i_D is equal to the SR discharge current i_{SR}. And the load current I_{out} consists of three parts, namely i_D, i_{S1} and i_{S2}. According to the current divider rule,

$$i_{S1} = -i_{S2} = \frac{C_r}{2C_r + C_{eq}} \cdot I_{out} \tag{2.2}$$

$$i_D = i_{SR} = \frac{C_{eq}}{2C_r + C_{eq}} \cdot I_{out} \tag{2.3}$$

where

$$C_{eq} = \frac{C_j \cdot C_{oss}}{C_j + C_{oss}} \tag{2.4}$$

Mode 1 ends when C_j is fully discharged to zero and then D_{Clamp} is forward biased. The time interval of mode 1 could be calculated as

$$t_1 - t_0 = \frac{V_{clamp} \cdot C_j}{i_{SR}} = \frac{V_{clamp} \cdot C_j}{C_{eq}/(2C_r + C_{eq}) \cdot I_{out}} \tag{2.5}$$

By the end of mode 1, the voltages across switch S_1, S_2 and SR are

$$v_{ds\_S1} = 0 + \frac{i_{S1} \cdot (t_1 - t_0)}{C_r} = V_{clamp} \cdot \frac{C_j}{C_{eq}} \tag{2.6}$$

$$v_{ds\_S2} = V_s - v_{ds\_S1} = V_s - V_{clamp} \cdot \frac{C_j}{C_{eq}} \tag{2.7}$$

$$\begin{aligned} v_{ds\_SR} = V_{in} - \frac{i_{SR} \cdot (t_1 - t_0)}{C_{oss}} &= V_{in} - V_{clamp} \cdot \frac{C_j}{C_{oss}} \\ &= V_s - V_{clamp} \cdot \frac{C_j}{C_{eq}} \end{aligned} \tag{2.8}$$

Mode 2 $(t_1 - t_2)$

This mode starts when D_{Clamp} starts conducting at the moment of t_1. Then, again, the load current I_{out} is divided into i_{S1}, i_{S2}, and i_{SR}, charging C_{r1} and discharging C_{r2} and C_{oss}; and i_{SR} is further divided into i_D and i_{diff}. In this mode, L_r is linearly discharged by V_{clamp}, thus

$$i_{Lr} = I_{out} - \frac{V_{clamp}}{L_r} \cdot (t - t_1) \tag{2.9}$$

$$i_{diff} = I_{out} - i_{Lr} = \frac{V_{clamp}}{L_r} \cdot (t - t_1) \tag{2.10}$$

The capacitor charging and discharging currents sum up to the load current I_{out}, and according to current divider rule,

$$i_{S1} = -i_{S2} = \frac{C_r}{2C_r + C_{oss}} \cdot I_{out} \tag{2.11}$$

$$i_{SR} = \frac{C_{oss}}{2C_r + C_{oss}} \cdot I_{out} \tag{2.12}$$

Then,

$$i_D = i_{SR} - i_{diff} = \frac{C_{oss}}{2C_r + C_{oss}} \cdot I_{out} - \frac{V_{clamp}}{L_r} \cdot (t - t_1) \tag{2.13}$$

When the voltage across S_2 and SR are discharged to zero and the body-diodes of both switches are forward biased, mode 2 ends. Meanwhile, S_1 voltage is charged to the voltage of V_s.

Mode 3 $(t_2 - t_3)$

The D_{Clamp} and the body diodes of S_2 and SR are conducting. L_r is still linearly discharged by V_{clamp} through D_{Clamp}. Thus, the currents in this mode are

$$i_{Lr} = i_{Lr}(t_2) - \frac{V_{clamp}}{L_r} \cdot (t - t_2) \tag{2.14}$$

$$i_D = i_D(t_2) - \frac{V_{clamp}}{L_r} \cdot (t - t_2) \tag{2.15}$$

$$i_{diff} = i_{diff}(t_2) + \frac{V_{clamp}}{L_r} \cdot (t - t_2) \tag{2.16}$$

$$-i_{S2} = i_{Lr}(t_2) - i_D(t_2) \tag{2.17}$$

$$i_{SR} = I_{out} - (-i_{S2}) = I_{out} - i_{Lr}(t_2) + i_D(t_2) \tag{2.18}$$

Mode 4 ($t_3 - t_4$ and $t_4 - t_5$)

S_2 and SR are turned on with ZVS at t_3. Then L_r is discharged by V_{clamp} through S_2 and SR. Meanwhile, SR current i_{SR} is increased to keep I_{out} constant. The current expressions for i_{Lr} and i_{SR} are

$$i_{Lr} = i_{Lr}(t_3) - \frac{V_{clamp}}{L_r} \cdot (t - t_3) \tag{2.19}$$

$$i_{SR} = i_{SR}(t_3) + \frac{V_{clamp}}{L_r} \cdot (t - t_3) \tag{2.20}$$

By the end of mode 4, the i_{Lr} is at a negative value and correspondingly, i_{S2} is positive. Since intervals (t_0 - t_2) and (t_5 - t_6) are the switching transition time, they are assumed very short compared to interval (t_2 - t_5) [26]. This assumption is valid even with 2.2 MHz switching frequency (19 ns transition time compared 230 ns on/off time observed in the prototype circuit). Then, based on the charge balance of the clamp capacitor (represented by the voltage source V_{clamp} in Figure 2.2),

$$i_c(t_5) = -i_c(t_2) \tag{2.21}$$

Since the clamp capacitor current is the same as the resonant inductor current, during t_2 to t_5, the resonant inductor current at t_5 is approximately

$$i_{Lr}(t_5) = i_c(t_5) = -i_c(t_2) = -i_{Lr}(t2) = -I_{out} \tag{2.22}$$

Mode 5 ($t_5 - t_6$)

At the moment of t_5, both S_2 and SR are turned off but SR is still conducting via its body-diode. Then the L_r starts to resonate with C_{r1}, C_{r2} and C_j. The current expressions in this mode could be found as

$$i_{Lr} = -I_{out} \cdot \cos(\omega(t - t_5)) - \frac{V_{clamp}}{Z} \cdot \sin(\omega(t - t_5)) \tag{2.23}$$

$$i_{S1} = i_{Lr} \cdot \frac{C_r}{2C_r + C_j} \tag{2.24}$$

$$i_{S2} = -i_{Lr} \cdot \frac{C_r}{2C_r + C_j} \tag{2.25}$$

$$i_D = -i_{Lr} \cdot \frac{C_j}{2C_r + C_j} \tag{2.26}$$

where

$$\omega = \frac{1}{\sqrt{L_r \cdot (2C_r + C_j)}}, \quad Z = \sqrt{\frac{L_r}{(2C_r + C_j)}} \tag{2.27}$$

Mode 5 ends when S_1 voltage falls to zero and its body-diode is forward biased. At the same time, C_{r2} voltage and C_j voltage are charged to V_s.

Mode 6 ($t_6 - t_7$)

Only the body-diodes of S_1 and SR are on and the other switches are off. The current through L_r rises linearly through the two body-diodes.

Mode 7 ($t_7 - t_8$ and $t_8 - t_9$)

At t_7, S_1 is turned on with ZVS and L_r continues being charged by the input voltage. The i_{Lr} and i_{SR} in modes 6 and 7 are

$$i_{Lr} = i_{Lr}(t_6) + \frac{V_{in}}{L_r} \cdot (t - t_7) \tag{2.28}$$

$$i_{SR} = I_{out} - i_{Lr} \tag{2.29}$$

The L_r is charged till its current i_{Lr} reaches the load current I_{out}, and correspondingly i_{SR} is reduced to zero with a slow slew rate. Then SR is turned off and mode 8 is started.

Mode 8 ($t_9 - t_{10}$)

At t_9, since the voltage at the drain side of SR is still zero, the L_r is still charged by the voltage across it, namely $V_{in} - v_{ds\_SR}$ or $v_{Dclamp} - V_{clamp}$. Then i_{Lr} is

$$i_{Lr} = I_{out} + \int \frac{V_{in} - v_{ds\_SR}(t)}{L_r} \mathrm{dt} \tag{2.30}$$

where $v_{ds\_SR}(t)$ is the instantaneous voltage across SR.

Meanwhile, the C_{oss} and C_j are charged and discharged in a resonant manner till v_{ds_SR} is increased to V_{in} and v_{Dclamp} is reduced to V_{clamp}. Then, ideally, this mode would end; but since the resonant inductor current i_{Lr} is larger than I_{out} at this moment, this extra current (energy) will cause a resonance between C_j, C_{oss} and L_r resulting in an oscillation as shown in Figure 2.3. During the resonance, the voltage across SR is clamped to V_s (if the resonant peak voltage is higher than V_s) and part of the extra energy in L_r will be recovered to the C_{clamp}. Also, if the resonant path impedance is low enough and the switching period is short (above MHz switching frequency), the oscillation will not be damped out and the energy will be saved.

2.3 Design Considerations

2.3.1 ZVS Analysis

From the above analysis of operating principle, it could be seen that the energy to achieve ZVS of S_2 and SR is from L_f. Therefore, it could be assumed that the ZVS range for S_2 and SR is from near-zero load to full load. However, for S_1, the energy

to realize ZVS operation comes from L_r. In mode 5, the switch S_1 voltage expression is determined by

$$\begin{aligned} v_{ds\_S1} = V_{in} + V_{clamp} \cdot \cos(\omega(t - t_5)) \\ -I_{out} \cdot Z \cdot \sin(\omega(t - t_5)) \end{aligned} \tag{2.31}$$

In order to achieve ZVS of S_1, the minimum value of V_{ds_S1} in (2.31) should be less than zero. Then it could be derived that

$$I_{out} \geq \sqrt{\frac{(2C_r + C_j) \cdot (V_{in}^2 - V_{clamp}^2)}{L_r}} \tag{2.32}$$

Therefore, for the given switches, resonant inductance and the input, there is a minimum load requirement for achieving ZVS operation of S_1.

2.3.2 Clamp Capacitor Requirement

During modes 3 and 4, the resonant inductor L_r actually resonates with the clamp capacitor C_{clamp}. To justify the assumption that C_{clamp} is approximately a constant voltage source, it is required that half of the $L_r - C_{clamp}$ resonance period should be much larger than the maximum of interval (t_2-t_5). Neglecting the switching transition time, interval (t_2-t_5) is the off time of S_1 during the operation. Therefore,

$$\pi \cdot \sqrt{L_r \cdot C_{clamp}} \gg (1 - D_{min}) \cdot T_s \tag{2.33}$$

where D_{min} is the minimum duty cycle of S_1 and T_s is the switching period.

Regarding the clamp capacitor voltage, from (2.14) and (2.19),

$$i_{Lr}(t_2) - i_{Lr}(t_5) = \frac{V_{clamp}}{L_r} \cdot (t_5 - t_2) \tag{2.34}$$

Then, it could be derived that,

$$V_{clamp} = L_r \cdot [i_{Lr}(t_2) - i_{Lr}(t_5)] \cdot (t_5 - t_2) = \frac{2L_r \cdot I_{out}}{(1-D) \cdot T_s} \tag{2.35}$$

In a proper design, V_{clamp} should be a relatively low value. This low voltage rating of C_{Clamp} benefits the use of small ceramic capacitors and commercial half-bridge drivers which can only withstand limited negative voltage on the source of high side switch.

2.3.3 Loss of Effective Duty Cycle

Another significant aspect of the proposed active clamp converter is that the modes 6 and 7 represent a loss of effective duty cycle. In several hundreds of kHz operation, this loss might not be significant but in MHz operation, the effective duty cycle loss cannot be ignored. The effective duty cycle in dc-dc converter is defined in terms of the charging and discharging cycles of the output filter inductor. As shown in Figure 2.5, during modes 6 and 7, the output filter inductor is still discharging and the loss of the duty cycle, ΔD can be derived as

$$\Delta D = L_r \cdot \frac{i_{Lr,peak} - i_{Lr,valley}}{V_{in} \cdot T_s} = \frac{2L_r \cdot I_{out}}{V_{in} \cdot T_s} \tag{2.36}$$

where $i_{Lr,peak}$ and $i_{Lr,valley}$ are the peak and valley values of i_{Lr}, respectively. Then the required duty cycle for given input/output voltage is

$$D = \frac{V_o}{V_{in}} + \frac{2L_r \cdot I_{out}}{V_{in} \cdot T_s} \tag{2.37}$$

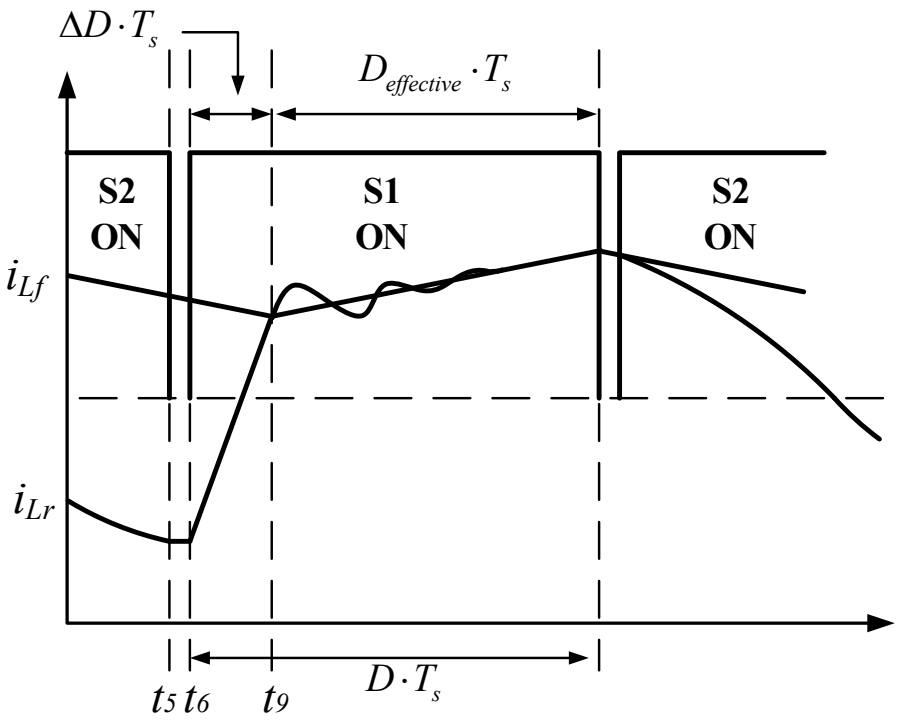


Figure 2.5: Waveforms Illustrating the Loss of Effective Duty Cycle.

2.4 Active-clamp Buck Converter Design

2.4.1 Design Specifications

Table 2.1 shows the specifications of a low power POL dc-dc converter for 14V PowerNet architecture. The static input voltage ranges from 8 V to 16 V, and the circuit should be able to withstand a transient input voltage up to 42 V. The switching frequency is 2.2 MHz which is well above the AM band.

2.4.2 Resonant Tank Design

For converters with ZVS turn-on, small capacitors added in parallel with the MOSFETs help to reduce the turn-off loss significantly. Therefore, a resonant capacitance of 1 nF (including the output capacitance of MOSFET) is added to both S_1 and S_2. Then the resonant inductance needs to be designed, which is related to three param-

Table 2.1: Design Specifications

Nominal Input Voltage	12-14 V
Static Input Voltage	8-16 V
Transient Input Voltage	up to 42 V
Output Voltage	5 V
Output Current	5 A
Switching Frequency	2.2 MHz

eters: maximum clamp capacitor voltage, maximum duty cycle, and ZVS range of switch S_1.

Figure 2.6 shows the ZVS range of S_1 at different input voltages with resonant inductance and load current as two variables, according to (2.32), (2.35) and (2.37). The ZVS range is designed for 8 V to 16 V input. Figure 2.6 indicates that, for ZVS down to half load at 16 V input, resonant inductance of at least 80 nH is required. Figure 2.7 shows the maximum duty cycles versus different input voltages, with inductance value as parameters. The inductance could not be arbitrarily large in order to keep duty cycle below one. Shown in Figure 2.8 is the clamp capacitor voltage versus different input voltages, at different values of inductance. Figure 2.8 indicates that the maximum clamp capacitor voltage limits the resonant inductance selection. Usually, the clamp capacitor voltage should be a relatively low value, if a bootstrap half-bridge driver is used for S_1 and S_2. In this design, the maximum clamp capacitor voltage is limited to 12 V.

Considering the limitations by maximum clamp capacitor voltage, maximum duty cycle, and the minimum ZVS range, the resonant inductance is selected as 80 nH.

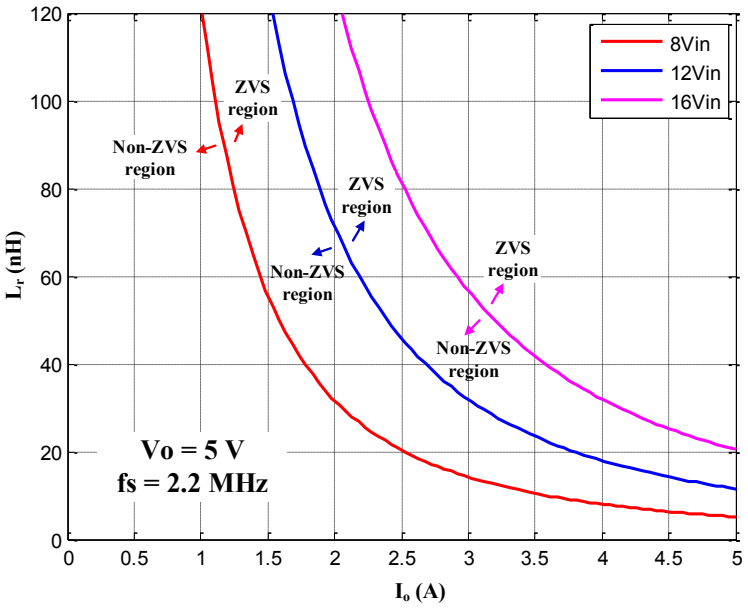


Figure 2.6: ZVS Range of S_1 at Different Input Voltages.

With this inductance value, the minimum load current to achieve ZVS of S_1 at 16 V input is around 2.5 A. When input voltage is lower, the minimum load current for ZVS is much reduced.

2.4.3 Clamp Capacitor Design

According to (2.33), with the designed parameters, the clamp capacitance should be much larger than 0.7 uF. The maximum clamp capacitor voltage is about 12 V as specified previously. Also, the maximum RMS current on the clamp capacitor is

$$I_{Cclamp,RMS}^{max} = \sqrt{\frac{1 - D_{min}}{3}} \cdot I_{out,max} \tag{2.38}$$

For this design, the maximum RMS current in the clamp capacitor is about 2.6 A.

2.4.4 MOSFET Switches Selection

For all the switches in this converter, the maximum blocking voltage is V_s, namely $V_{in} + V_{clamp}$. Figure 2.9 shows the plot of V_s versus input voltage covering the entire

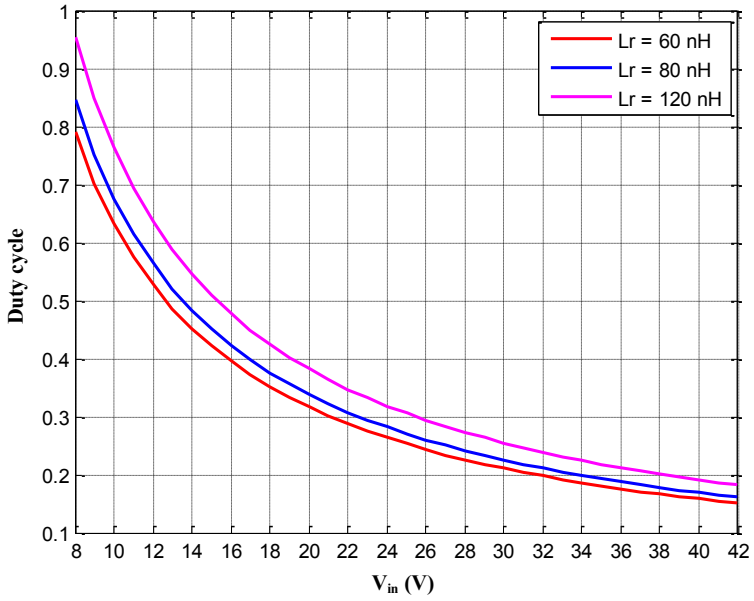


Figure 2.7: Plot of Duty Cycle versus Input Voltages.

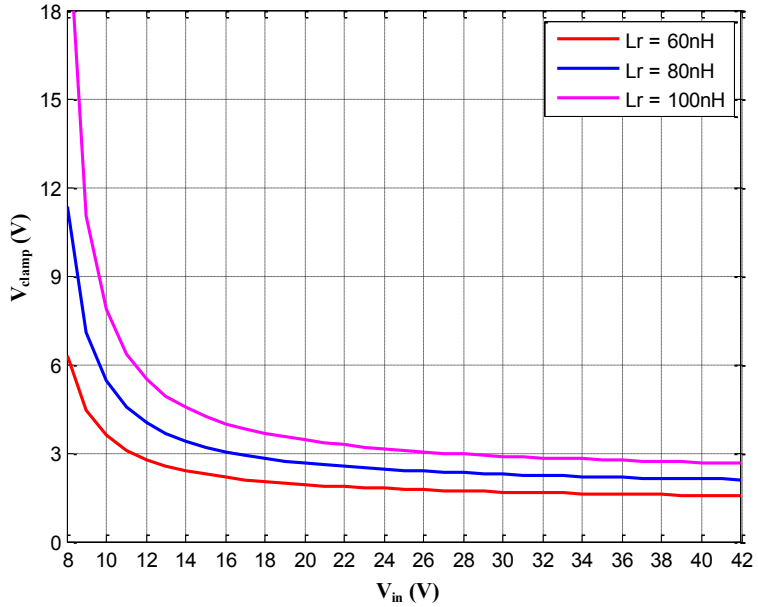


Figure 2.8: Plot of V_{clamp} versus Input Voltages.

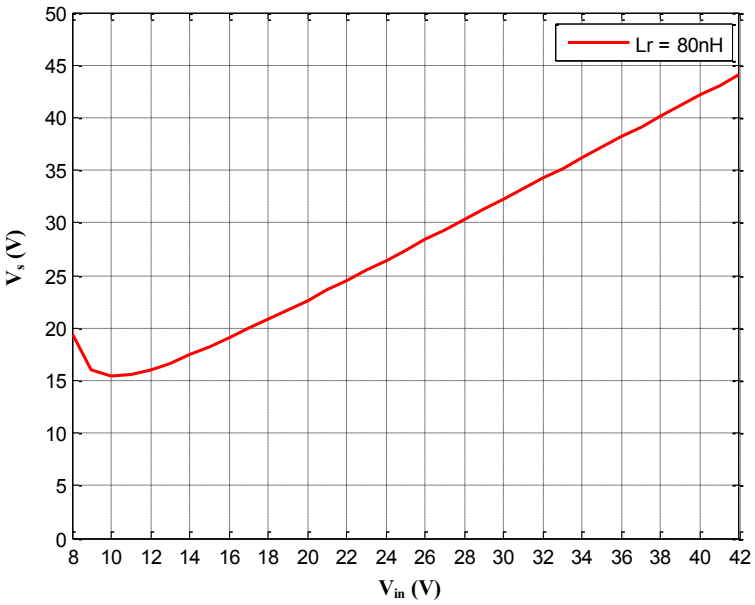


Figure 2.9: Plot of V_s versus Input Voltages.

range of operation. It could be seen the high clamp capacitor voltage occurs at low input voltage. Thus, with 42 V maximum input, the maximum V_s voltage is only about 44 V with 80 nH resonant inductance. Therefore, considering safety margin, 60 V MOSFETs are adequate for all the switches.

The maximum RMS current through S_1 occurs at maximum load and minimum input voltage, and is given by

$$I_{S_1,RMS}^{max} = \sqrt{D_{eff,max} + \frac{\Delta D_{max}}{3}} \cdot I_{out,max} \tag{2.39}$$

where $D_{eff,max}$ is the maximum effective duty cycle, and ΔD_{max} is the corresponding duty cycle loss. While for S_2 and SR, the maximum RMS current occurs at maximum load and maximum input voltage, and are derived as

$$I_{S_2,RMS}^{max} = \sqrt{\frac{1 - D_{min}}{3}} \cdot I_{out,max} \tag{2.40}$$

$$I_{SR,RMS}^{max} = 2\sqrt{\frac{1 - D_{min} + \Delta D}{3}} \cdot I_{out,max} \tag{2.41}$$

Table 2.2: Key Components Selection and Values for 2.2 MHz Active-clamp Buck Converter

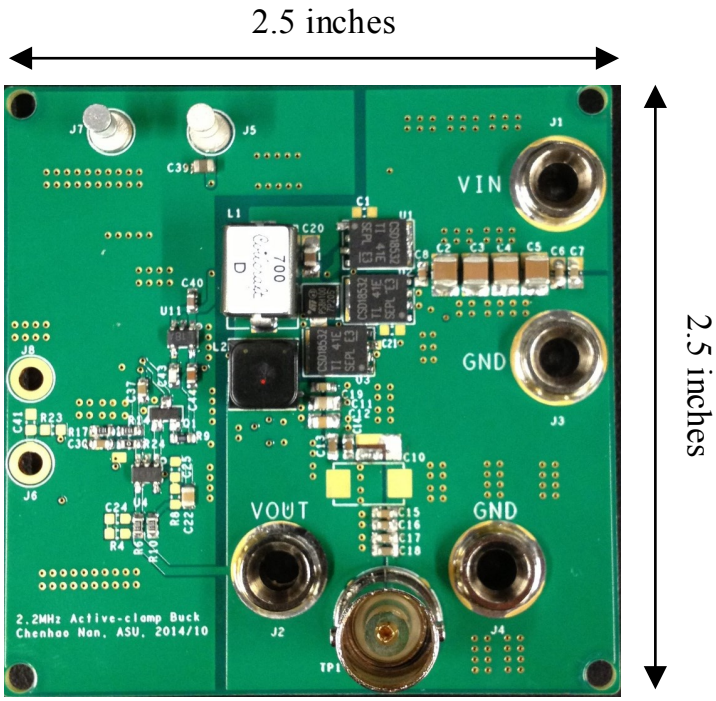
Components	Value/Part Number	Description
MOSFETs S_1, S_2 and SR	BSC097N06NS	60V, 10mΩ @ $8V_{gs}$
Clamp Diode D_{clamp}	STPS8H100DEE	schottky, 100V, 8A
Resonant Inductor L_r	Coilcraft SLC1175-700	0.252mΩ DCR, 78nH @ 2MHz
Filter Inductor L_f	Coilcraft EPL7040-152	1.5uH, 6.2mΩ DCR
Clamp Capacitor C_{clamp}	3.3 uF	ceramic cap, 25V
Filter Capacitor C_o	115 uF	68uF polymer cap + ceramic caps

In this design, the maximum RMS currents of S_1, S_2 and SR are about 4.6 A, 2.6 A and 5.3 A, respectively.

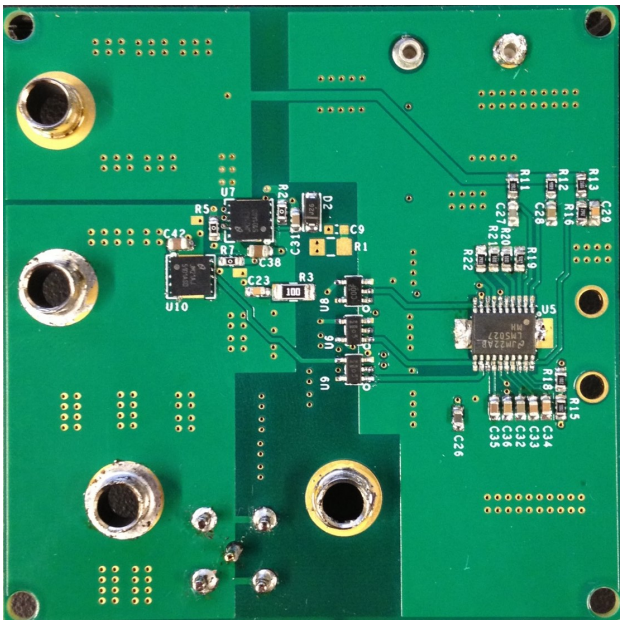
2.5 Experimental Verification with Si Devices

2.5.1 Hardware Implementation

As a proof-of-concept, a 2.2 MHz prototype converter has been built, as shown in Figure 2.10. The schematic and layout design are shown in Appendix A. Table 2.2 shows the components selection and key parameters. A half-bridge driver is employed to drive S_1 and S_2, for low cost and high density design. SR is driven by another low side driver for better timing control (such as adaptive delay control in future work) although it could also use the gate signal for S_2 and save one driver. In addition, LM5027 is employed as the PWM controller and simple voltage-mode control is used for output regulation.



(a) top side



(b) bottom side

Figure 2.10: 2.2 MHz Active-clamp Buck Converter Prototype.

2.5.2 Experimental Results

Figure 2.11 and 2.12 show the switching waveforms of S_1 and S_2 at 12V input, 5V/2.5A output. It could be seen that both S_1 and S_2 can realize ZVS turn-on. Also, with the added small capacitor in parallel, the turn-off transition is also nearly ZVS. In addition, the dv/dt (of V_{ds} waveforms) for all the switches is only around 0.75 V/ns. This is significantly lower than the dv/dt in a high efficiency hard-switching buck converter. Therefore, the EMI noise could be much lower. Figure 2.13 shows the switching waveforms of SR. It has ZVS turn-on as well and ZCS turn-off. It should be noted that a slow turn-off (equivalent to a fixed turn-off delay) is employed for SR to reduce SR body-diode conduction time and hence the power loss. For comparison, the switching waveforms of SR without the diode clamp is also shown in Figure 2.13. It can be seen that the voltage spike without the clamp diode is huge. Shown in Figure 2.14 is the voltage across D_{Clamp}. It could be seen that there is some ringing in the waveforms after SR is turned off. Since the converter is operating at 2.2 MHz and it is sensitive to the resonant inductance, the L_r current measurement with a wire is not feasible. Instead, the voltage across L_r could be measured and then the inductor current waveform could be derived, as shown in Figure 2.16. The derived i_{Lr} waveform is close to the analytical waveform shown in Figure 2.3.

2.5.3 Loss Analysis and Breakdown

Figure 2.17 shows the measured efficiency at different input voltages, with and without control and driver loss included. The control and driver power is derived from a separate source and its power is measured as 0.72 W separately. At nominal 12 V input, peak efficiencies of 93.5% and 89.7% are realized without and with driver and control loss included, respectively. It could be seen from Figure 2.17 that the

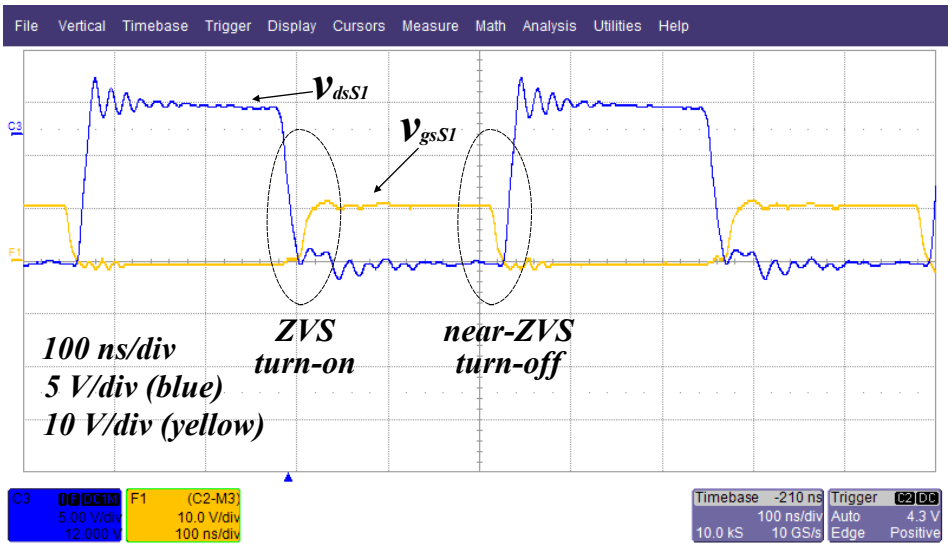


Figure 2.11: Switching Waveforms of S_1.

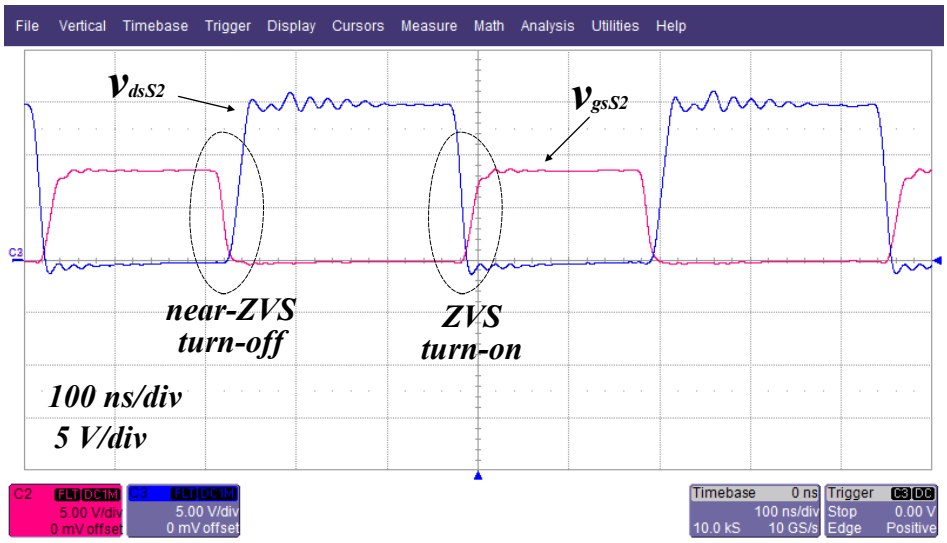


Figure 2.12: Switching Waveforms of S_2.

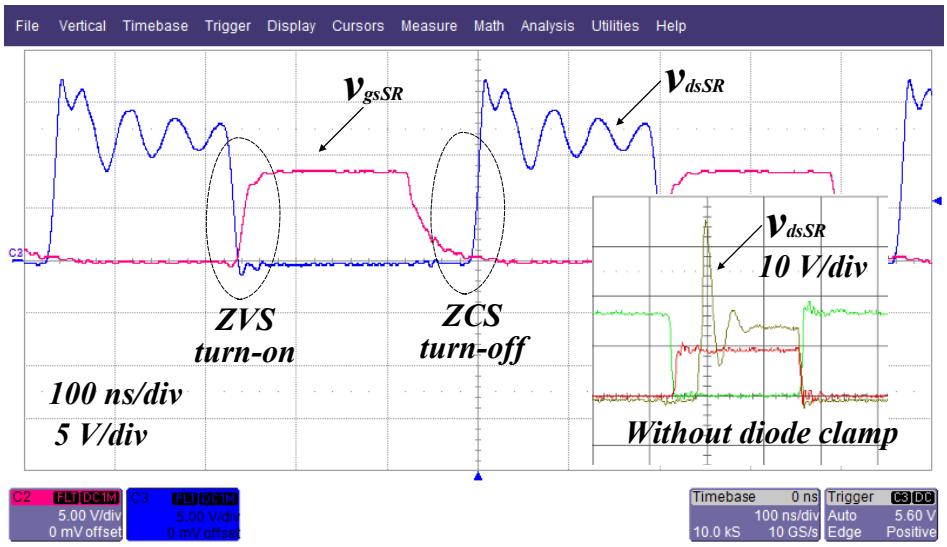


Figure 2.13: Switching Waveforms of SR.

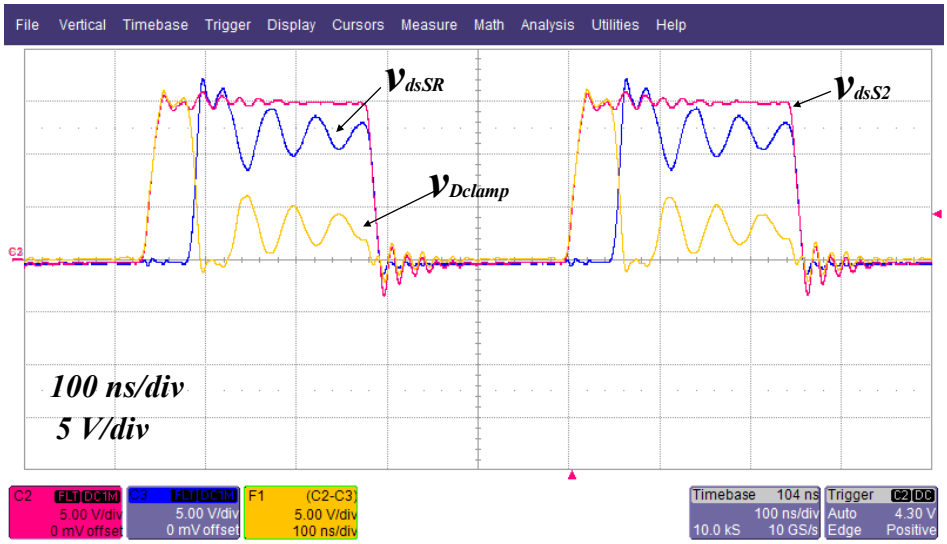


Figure 2.14: Switching Waveforms of Clamp Diode D_{clamp}.

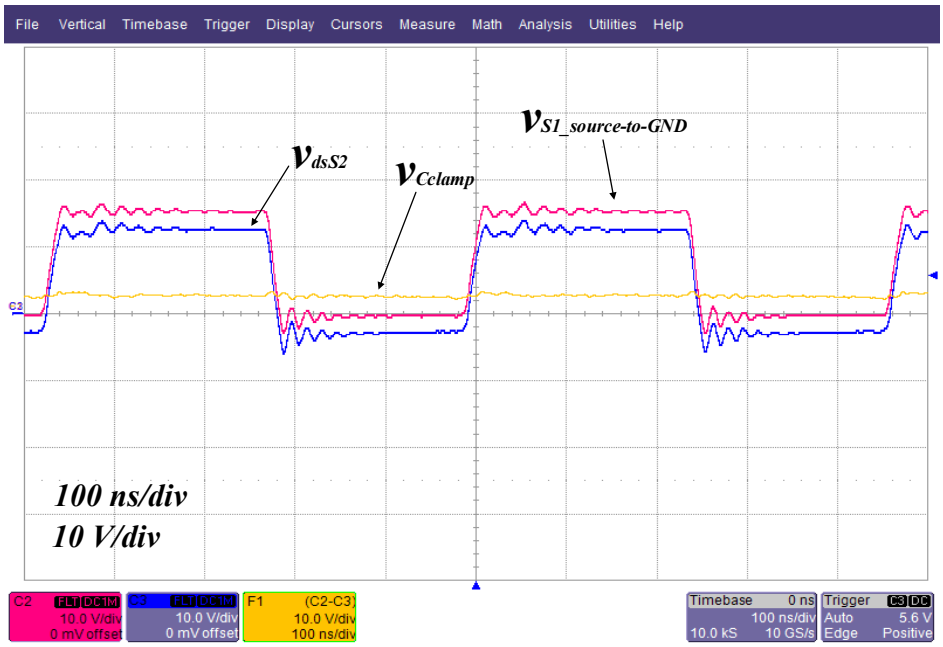


Figure 2.15: Voltage on Clamp Capacitor C_{clamp}.

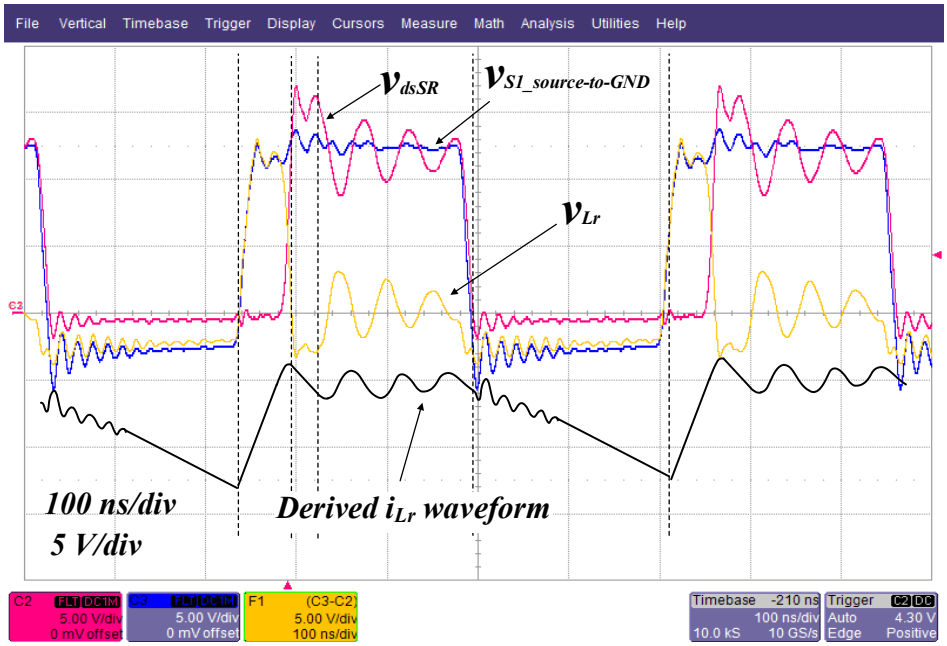


Figure 2.16: Voltage Waveform across the Resonant Inductor L_r and Derived Resonant Inductor Current Waveform.

efficiency with driver and control loss included is much lower than that without driver and control loss included. This is because the driver and control loss is actually the biggest part among all the losses, as shown in Figure 2.19. Figure 2.18 shows the experimental efficiency comparison between the proposed active-clamp buck converter and the conventional synchronous buck converter, at 12 V input and 5 V output. It is indicated that, within most part in the load range, the total efficiency (including driver and control loss) is improved by 1% to 3%. Moreover, in order to reduce switching losses, the dv/dt rate of the switching (dv/dt of v_{ds} waveforms) in conventional buck converter is much higher than that in the active-clamp buck converter, degrading the EMI performance. The lower dv/dt of v_{ds} in soft switching converters improves the EMI performance without the penalty of increasing the switching losses. Figure 2.19 is the calculated relative contribution of losses at 12 V input and 5 V output, for the proposed active-clamp buck converter. The calculation takes into account the conduction losses, switching losses, gate drive losses, body diode losses, magnetic losses, etc. The total calculated power losses under different operating conditions are corrected to experimental results under the same operating conditions as a means of calculation validation. The reason for large drive loss is that the minimum V_{dd} voltage for the specific driver used was 8 V leading to minimum gate voltage of 8 V. If a driver IC with 5 V minimum V_{dd}, and therefore, gate voltage at 5 V, can be used the efficiency can be further improved. From a detailed loss analysis considering the increased MOSFET on-state resistance at lower gate voltage, efficiency improvement in going from 8 V gate drive to 5 V gate drive was calculated to be from 89.7% to 91.3%, at 12 V input and 5 V output.

Shown in Figure 2.20 is the calculation/simulation based efficiency comparison of the proposed active-clamp buck converter and other active-clamp based buck converters. Only the power stage efficiencies are compared here. It clearly shows that

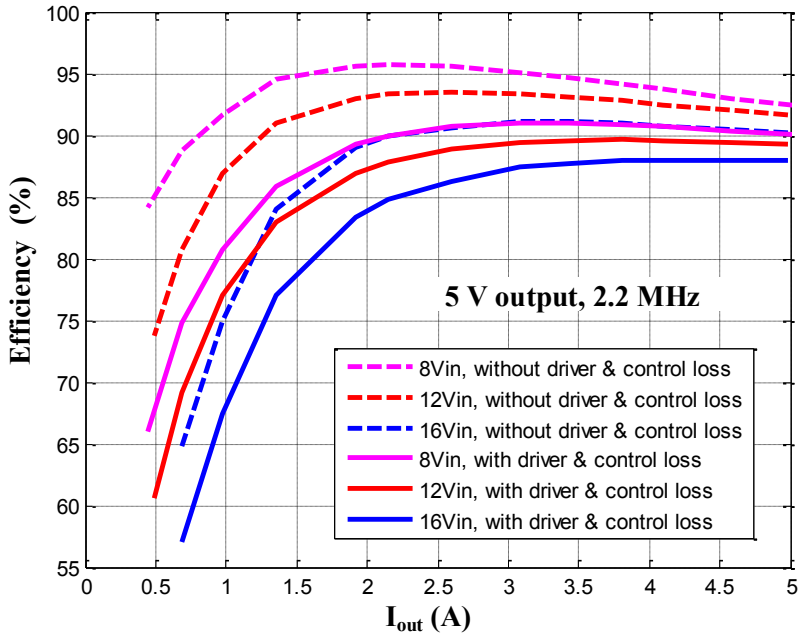


Figure 2.17: Measured Efficiency Curves of Active-clamp Buck at 8 V, 12 V and 16 V Inputs, Respectively.

the efficiency of the proposed converter is higher by 0.5% - 2%. This is because all other previously proposed active-clamp based buck converters employ no voltage spike clamping or lossy voltage spike clamping for the synchronous output rectifier. The overall efficiency is hence impacted. In addition, the active-clamp buck with coupled-inductor, compared to the converter with separated inductors, has more conduction loss in the magnetic windings although the core loss is reduced. Also, the conduction loss in synchronous rectifier is much increased due to larger RMS current.

2.6 Employment with GaN Devices

2.6.1 Motivation of Using GaN Devices

One potential solution to improve the efficiency is to employ the GaN FETs that feature lower capacitances and $R_{ds,on}$ compared to its silicon counterparts [48–52]. In some applications, such as in the voltage regulator, the application of GaN devices

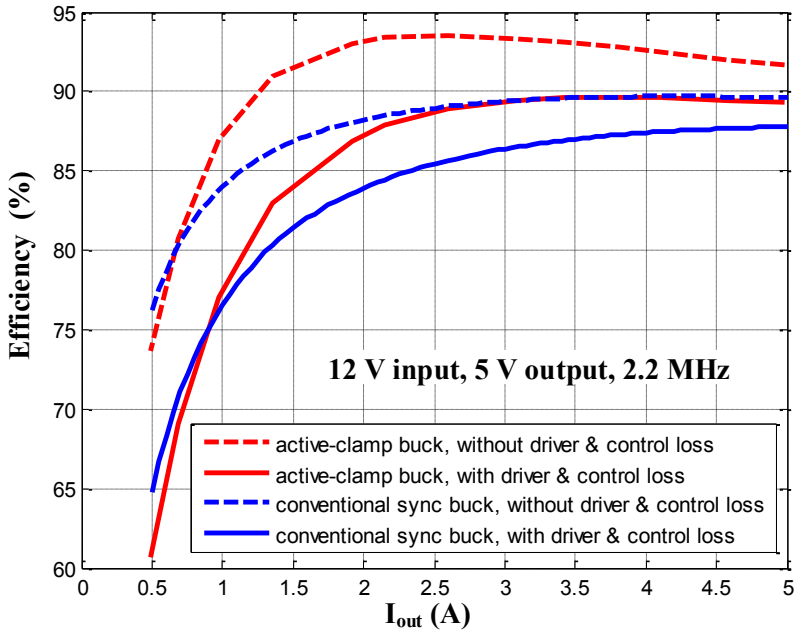


Figure 2.18: The Comparison Efficiency v.s. Load between the Active-clamp Buck and Conventional Synchronous Buck Converter, at 12 V Input and 5 V Output.

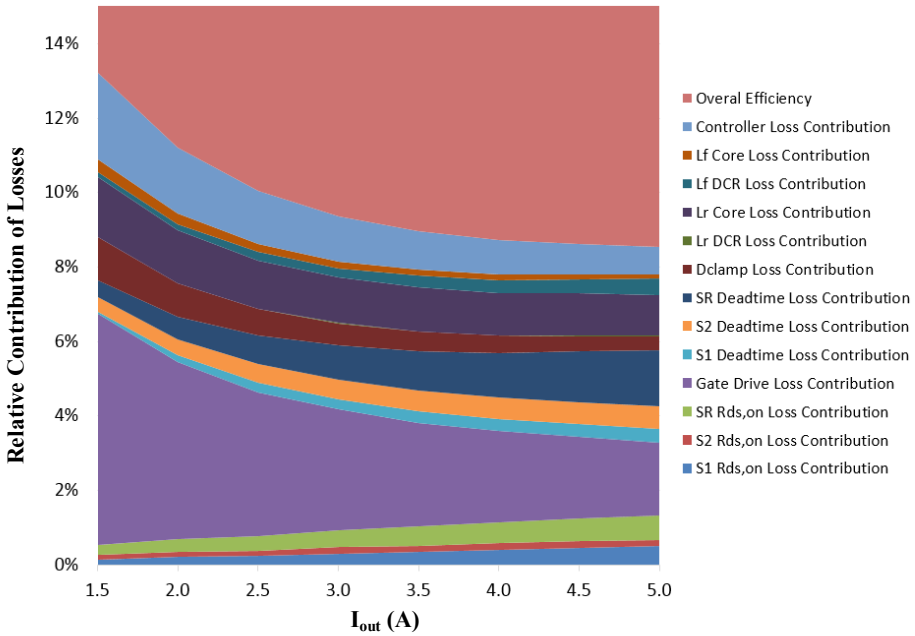


Figure 2.19: Analytical Loss Break Up at 12 V Input.

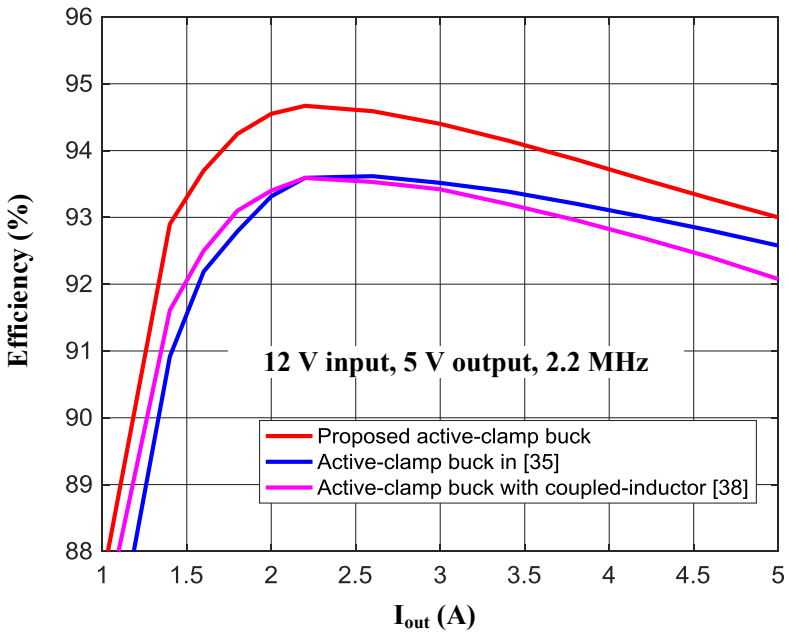


Figure 2.20: Efficiency Comparison between Proposed Active-clamp Buck and Other Active-clamp Based Buck Converters.

has demonstrated significant efficiency improvement over the Si MOSFET based regulators [53]. This is because the GaN FETs with lower capacitances can switch much faster than Si MOSFET; thereby the switching loss in buck converter is much reduced. However, for automotive POL converters, the switching transition speed is usually limited by EMI consideration and could not be arbitrarily reduced. Automotive buck converters cannot fully utilize the capability of fast switching provided by GaN devices and hence the efficiency improvement with GaN devices might not be significant. This is part of the motivation of using the soft-switching converter to improve the efficiency. With the ZVS operation, the switching transition speed is not critical and does not impact the efficiency. However, the trade-off of no switching loss in soft-switching topologies is usually higher RMS current in switches. With Si MOSFET, the conduction loss is considerable. More importantly, the Si MOSFETs with low $R_{ds,on}$ usually have large C_{iss} and hence Q_g. Thus, the gate drive loss at

Table 2.3: Key Parameters of Several Best-in-class 60 V to 100 V Si and GaN Devices

Devices		V_{DS}	$R_{ds,on}$	Q_g
Si MOSFET (V_{gs} = 6 V)	BSC097N06NS	60 V	12 mΩ	7.5 nC
	BSC039N06NS	60 V	4.8 mΩ	16.2 nC
	BSC160N10NS3 G	100 V	17.6 mΩ	11.4 nC
GaN FET (V_{gs} = 5 V)	EPC2001C	100 V	5.6 mΩ	7.5 nC
	EPC2016C	100 V	12 mΩ	3.4 nC

high switching frequency is very significant. This has been noticed from the loss breakdown of the Si based prototype. However, the GaN FETs with same $R_{ds,on}$ have much smaller C_{iss} than Si MOSFET and then the gate driver loss could be much saved. Another benefit of GaN FETs, when using resonant gate driver, is much smaller internal gate meshed resistance R_G. For Si MOSFETs, R_G usually ranges from 1 Ω to 2 Ω; while for EPC GaN FETs, R_G is only 0.3 Ω to 0.4 Ω. Usually it is hard to achieve high efficiency of resonant gate driver with large R_G. In summary, the combination of GaN FETs and soft-switching topology for automotive low power POL converters could be promising [54].

Table 2.3 shows the key parameters of several best-in-class 60 V to 100 V Si MOSFETs and GaN FETs. It could be seen that the 100 V GaN devices either have lower $R_{ds,on}$ or lower Q_g compared to 60 V Si MOSFET. The advantages of 100 V GaN FET are more significant over 100 V Si MOSFET. Thus it could be concluded that the employment of GaN devices can further improve the efficiency of the proposed active-clamp buck converter for low power automotive applications.

Table 2.4: Key Parameter Values and Components Selection

Components/Parameters	Values
Resonant Capacitor C_r	1.3 nF
Resonant Inductor L_r	80 nH
Clamp Capacitor C_{clamp}	3 uF
MOSFET S_1, S_2 and SR	EPC2001C
MOSFET Driver	LM5113
Schottky Diode Paralleled with GaN FETs	DFLS160-7
Clamp Diode D_{clamp}	DFLS160-7

2.6.2 Hardware Implementation

The design specification is the same as that for Si devices, as shown in Table 2.1. The key parameters and components selection for GaN based prototype is shown in Table 2.4. The schematic and layout design are shown in Appendix B.

As shown in Table 2.4, EPC enhancement-mode GaN (eGaN) FET EPC2001 is selected as the switches in this converter. The implementation with eGaN FET is very challenging. One challenging is the gate driver design that should make the driver loop stray inductance minimized [55]. This is because once the gate voltage ringing is higher than 6 V, the gate of EPC eGaN FET will be damaged. The layout of the gate drive loop for all switches are shown in Figure 2.21 and 2.22. The red (solid and dashed) lines indicate the turn-on path and the orange (solid and dashed) line indicate the turn-off path. Physically, the loops are minimized by layout. To accurately estimate the stray inductance in the path, the ANSYS Q3D is used to

simulate the parasitic parameters of the driver loop path and the results are shown in Table 2.5. Since the stray inductance in S_1 and S_2 drive loops is large enough to make ringing higher than 6 V, external gate resistors of several ohms are needed to damp the resonance between L_{stray} and C_{gs}. Because of ZVS turn-on, the relative slow turn-on speed due to external resistance would not impact the switching loss and hence the efficiency.

In addition, to minimize the stray inductance associated loss in the power loop, the layout of the high frequency power loop $C_{in} - S_1 - C_{clamp} - S_2 - GND - C_{in}$ is optimized [56]. The ANASYS Q3D simulation result shows that the stray inductance in this loop is only 0.776 nH.

Another issue special to eGaN FET is the relatively large reverse conduction voltage drop, such as 1.8 V with 0.5 A reverse current. The deadtime for eGaN devices should be minimized to reduce the large reverse conduction loss, or adaptive gate driver could be used to further avoid the reverse conduction loss [57]. In this design, Schottky diodes with minimized package inductance are selected to be in parallel with each eGaN FET, in order to avoid eGaN reverse conduction loss.

The built 2.2 MHz prototype of the GaN based active-clamp buck converter is shown in Figure 2.23.

2.6.3 Experimental Results

Figure 2.24 and 2.25 show the switching waveforms of S_1 and S_2 at 12 V input, 5V/2.5A output. It could be seen that both S_1 and S_2 can realize ZVS turn-on. Also, with the added small capacitor in parallel, the turn-off transition is also nearly ZVS. In addition, the dv/dt for all switches is only around 0.7 0.75 V/ns. Figure 2.26 shows the switching waveforms of SR. It has ZVS for both turn-on and turn-off. Shown in Figure 2.27 is the voltage across the clamp diode. Figure 2.28 shows the

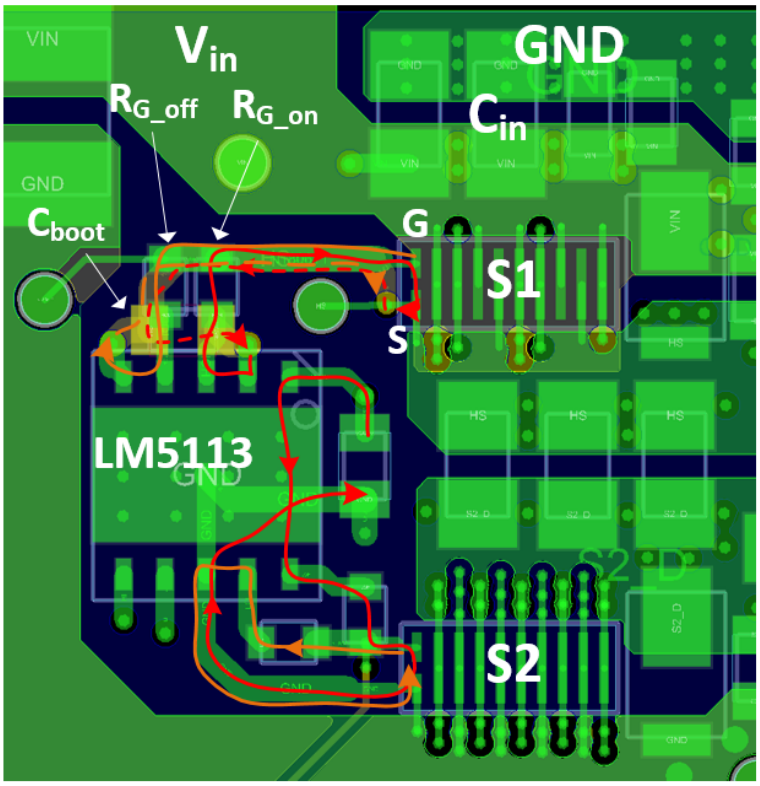


Figure 2.21: Layout Design of S_1 and S_2 Driver Loop.

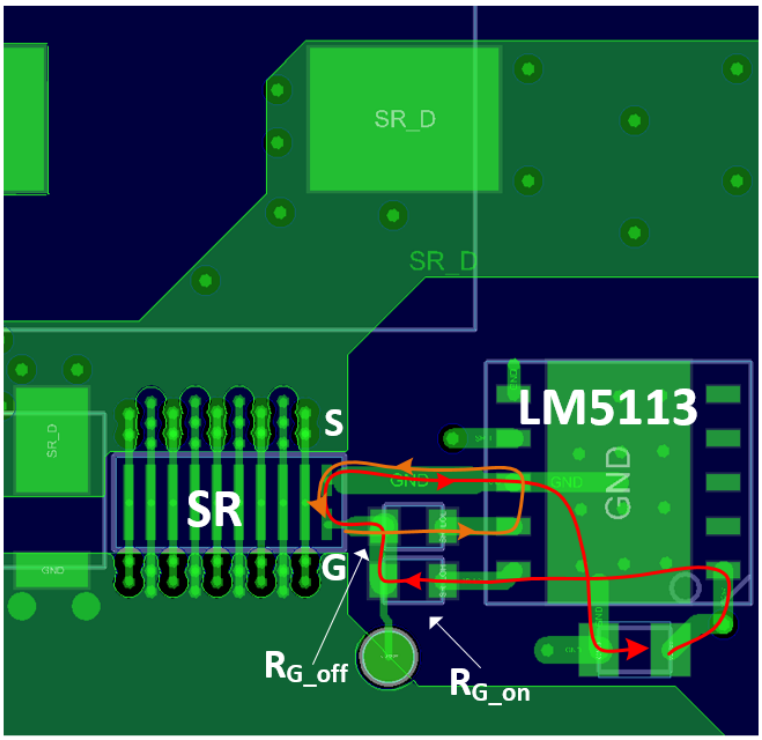
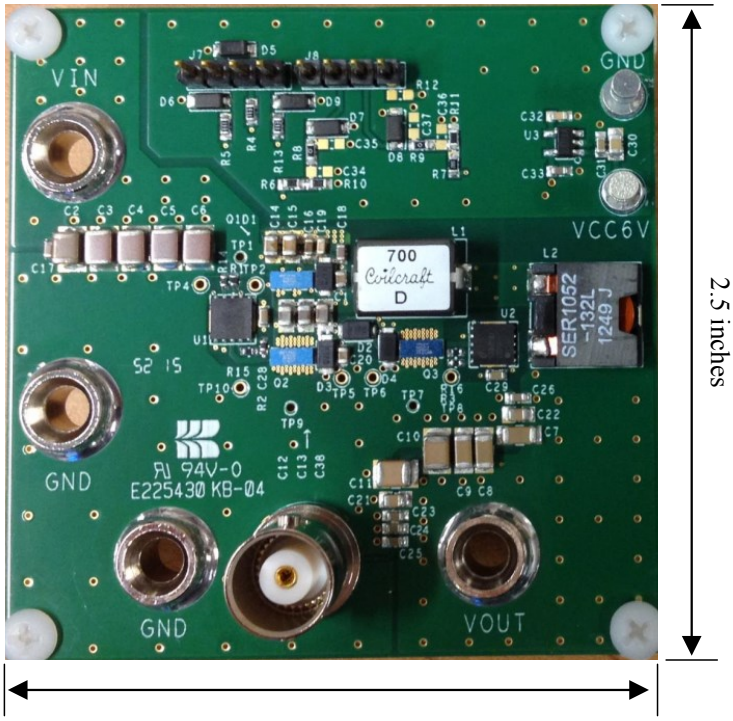
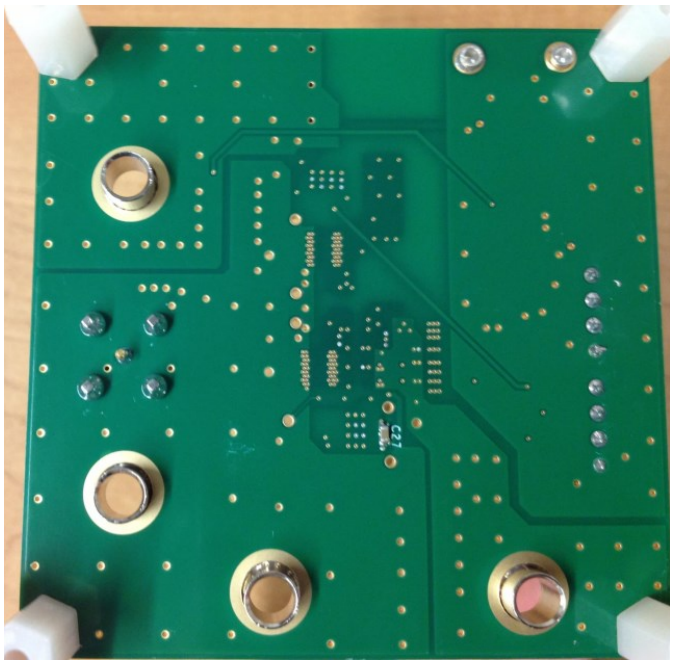


Figure 2.22: Layout Design of SR Driver Loop.



(a) top side



(b) bottom side

Figure 2.23: Prototype of 2.2 MHz GaN Based Active-clamp Buck Converter.

Table 2.5: Q3D Simulation Results

	L_{stray} (nH)	R_{stray} (mΩ)
S_1 turn-on loop	6.08	13.20
S_1 turn-off loop	6.29	9.69
S_2 turn-on loop	3.40	11.69
S_2 turn-off loop	2.09	6.97
SR turn-on loop	2.64	10.31
SR turn-off loop	1.16	4.49

voltage across the resonant inductor.

Figure 2.29 shows the efficiency comparison between using GaN FETs and Si MOSFETs. It should be noted that, for both prototypes, the SR is turned off at the same time of S_2 turn-off. Figure 2.29 indicates that, without considering control and driver loss, the efficiency improvement from GaN FETs is from 0.5% to 3%. However, when considering the driver and control loss, GaN based prototype shows much higher efficiency than Si based prototype efficiency. This is because with the same on-resistance, the gate charge of GaN FET is smaller than that of Si MOSFETs. Also, considering the V_{gs} voltage difference (5 V vs. 8 V), the gate driver loss is much reduced in GaN FETs based converter. Even assuming 5 V V_{dd} for Si based prototype, the calculated peak efficiency is only 91.3% at 12 V input and 5 V output.

2.6.4 SR Turn-off Time Optimization

It has been pointed out that the SR deadtime loss is a major part among the total losses. The deadtime here means the interval between the turn-off of SR channel and

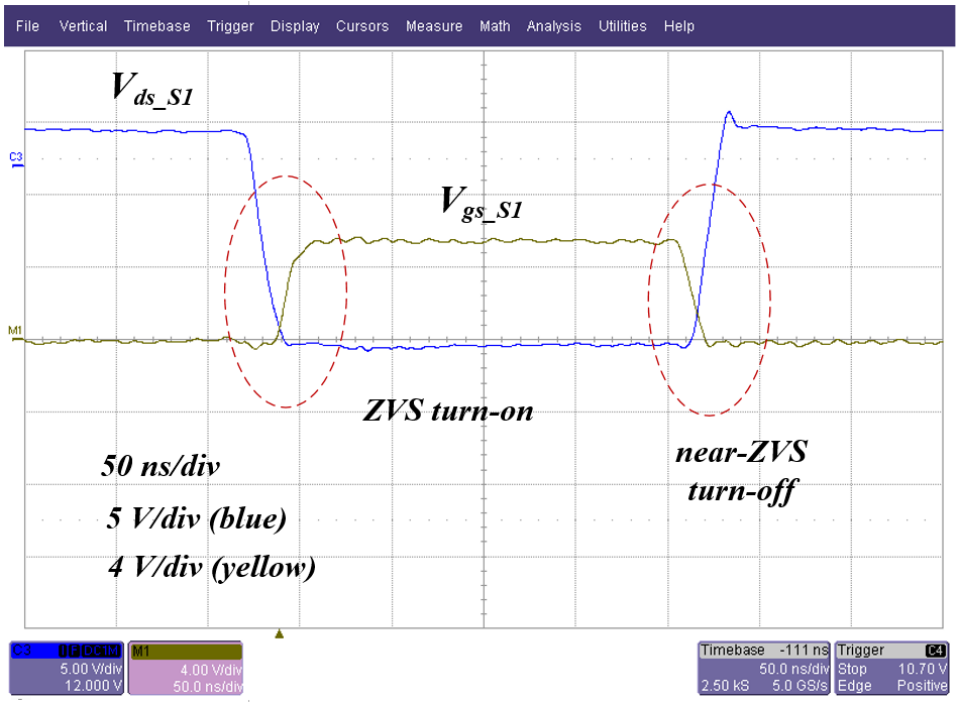


Figure 2.24: Switching Waveforms of S_1.

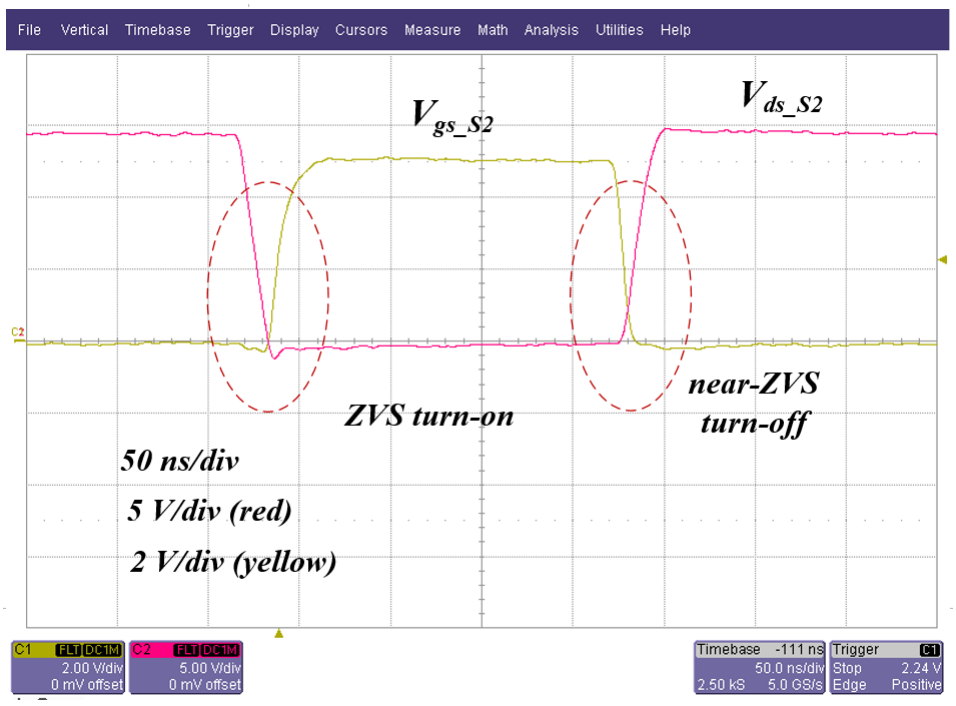


Figure 2.25: Switching Waveforms of S_2.

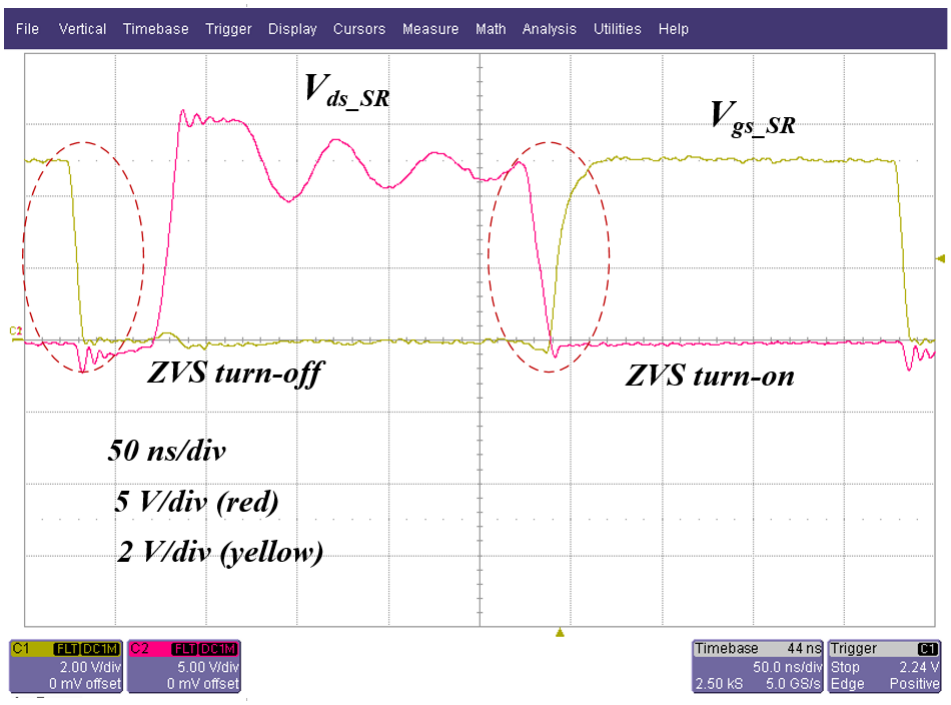


Figure 2.26: Switching Wavefroms of SR.

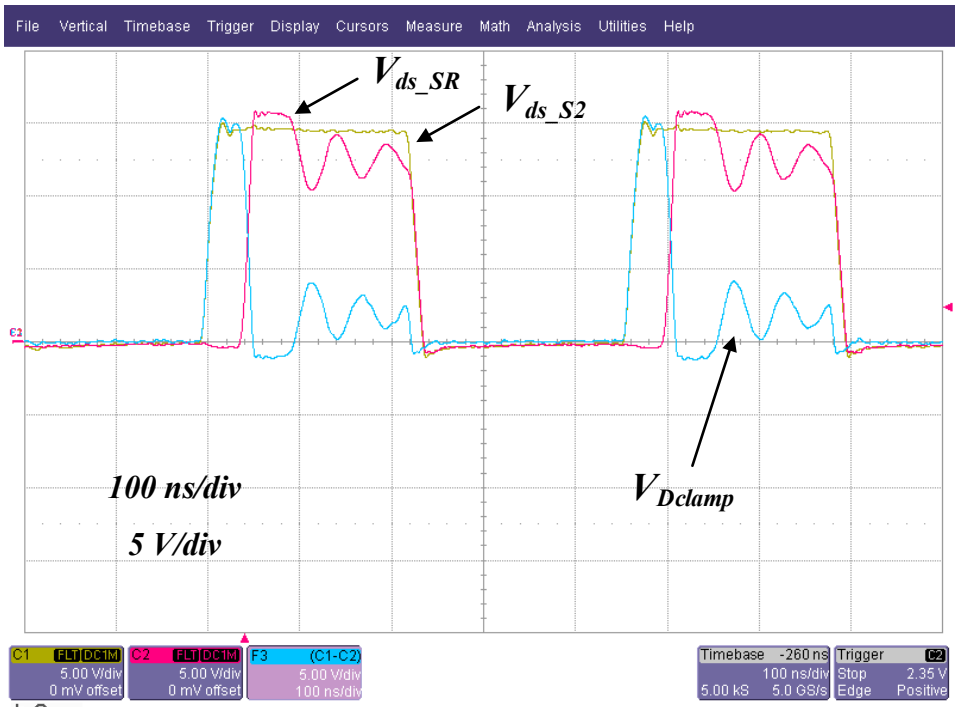


Figure 2.27: Voltage Waveform across the Clamp Diode.

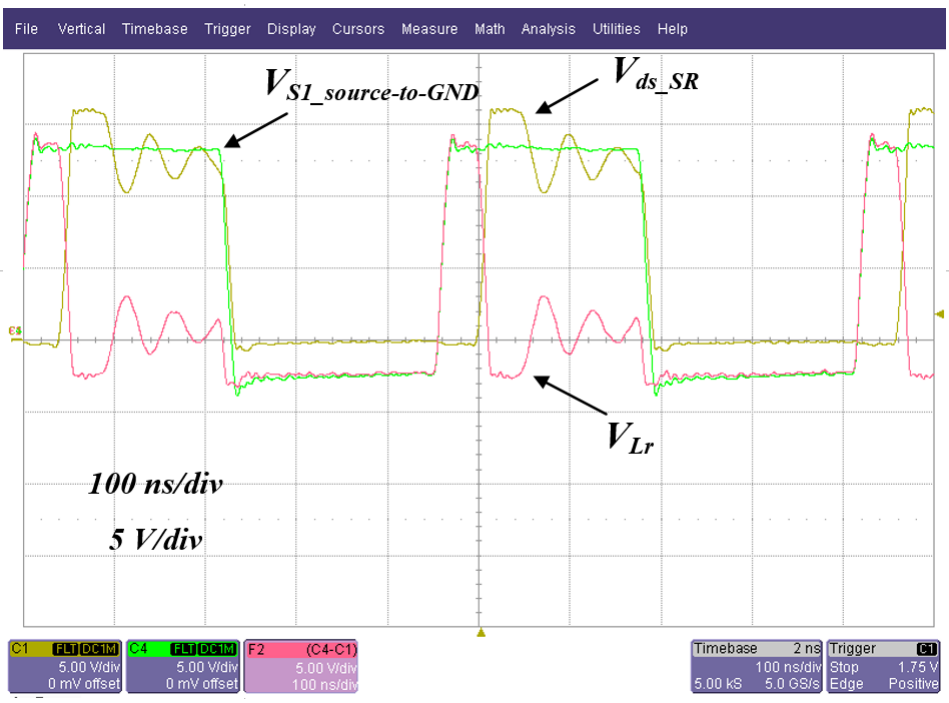


Figure 2.28: Voltage Waveform across the Resonant Inductor.

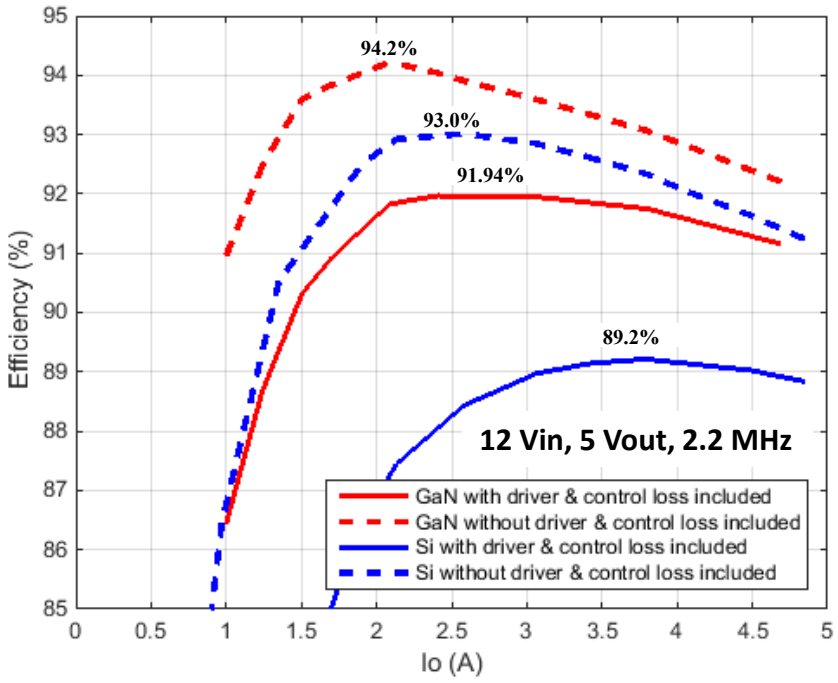


Figure 2.29: Efficiency Comparison between Using Si MOSFETs and GaN FETs.

the turn-off of SR body-diode. If the SR is turned off at the same time as S_2 turn-off, the SR body-diode will conduct current with an average value of I_o for $\Delta D \cdot T_s$. Thus, the conduction loss in SR body-diode is considerable. With the digital control used in GaN FETs based prototype, it is easier to delay the turn-off of SR to reduce its conduction loss. The problem is to find an optimized delay time for SR turn-off, and under different operating conditions, this optimized delay time varies. Two methods (measurement and calculation, and measurement results are used to calibrate the calculation algorithm) are employed together to help find this optimized delay. First, several SR turn -off delay times are used and the corresponding efficiencies are measured. For example, Figure 2.30 shows the efficiency curve with different SR turn-off delay times on 12 V input, 5 A load condition. By interpolation based on the tested data, the SR turn-off delay leading to highest efficiency could be read. Similarly, for other load conditions, the optimized delay time (maximum efficiency) could be measured, as shown in Table 2.6. This table also shows the calculated optimized SR turn-off delay. The calculation is based on the assumption that the highest efficiency occurs when the SR turns off at the moment that resonant inductor current reaches filter inductor current. Figure 2.31 illustrates the optimized SR turn-off delay in two cases: ZVS of S_1 is achieved and not achieved. Based on the equations describing the converter operation, the delay time could be calculated. Table 2.7 and Table 2.8 show the measured optimized delay and calculated delay for SR turn-off at 8 V and 16 V inputs, respectively. From tables 2.6, 2.7 and 2.8, it could be seen that the calculated delay time is close to the measured SR turn-off delay time.

However, the calculation method used above involves the equations describing the converter operation. It is hard to be used for adaptively changing the SR turn-off delay in real-time. Therefore, a simplified calculation algorithm is needed for implementation.

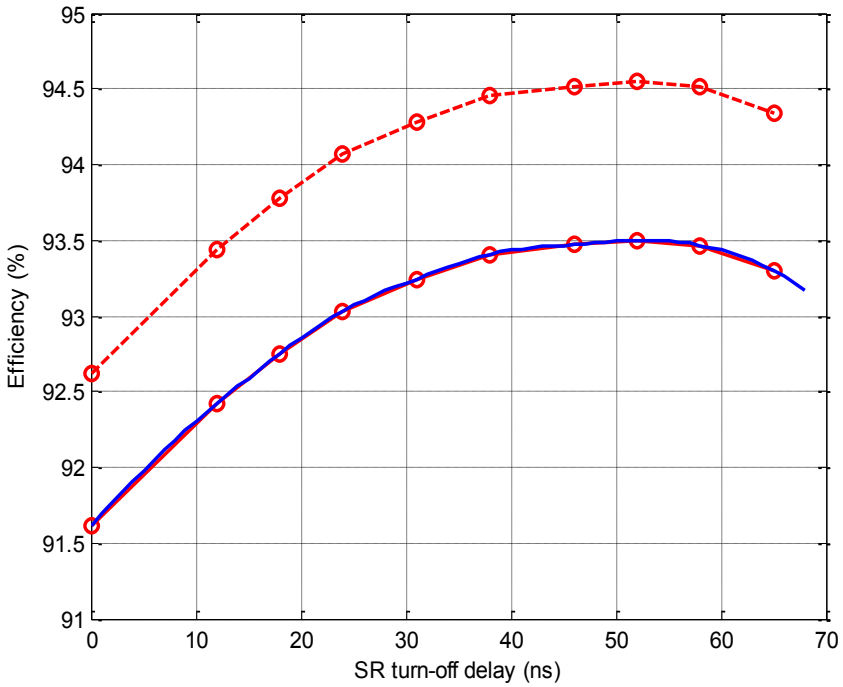


Figure 2.30: Efficiency Curve with Different SR Turn-off Delay at 12 V Input, 5 A Load.

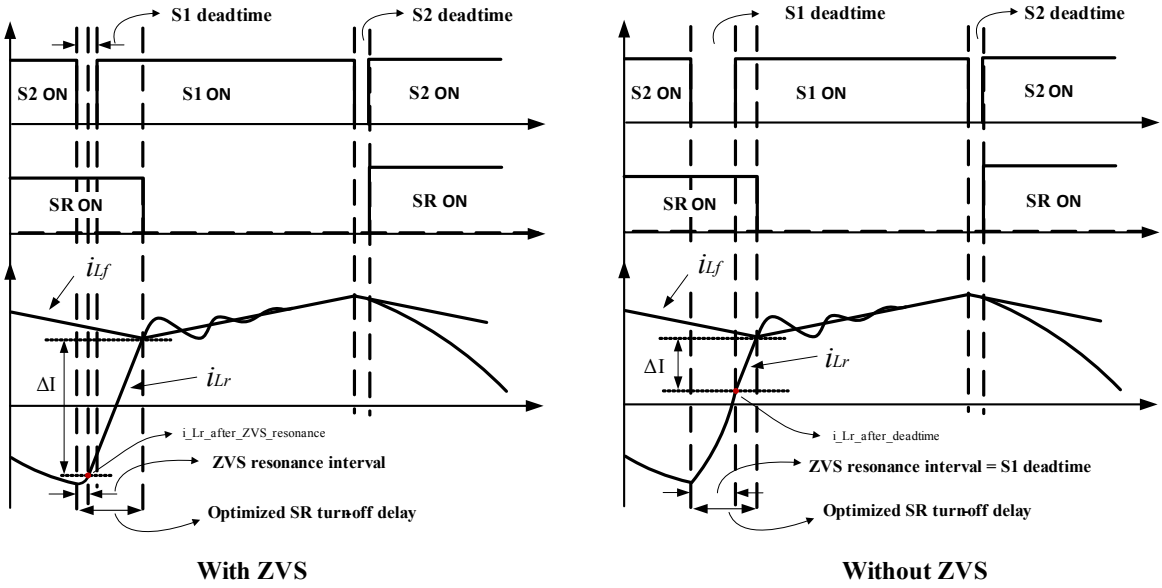


Figure 2.31: Waveforms Illustrating Optimized SR Turn-off Delay.

Table 2.6: Measured Optimized SR Turn-off Delay Time at 12 V input

V_{in}	I_o	Measured Efficiency	Measured Optimal SR Turn-off Delay	Calculated Optimal SR Turn-off Delay
12 V	4.95 A	93.00%	58 ns	64 ns
12 V	4.5 A	93.10%	53 ns	59.8 ns
12 V	4.01 A	93.13%	46 ns	52.8 ns
12 V	3.51 A	93.22%	42 ns	47.7 ns
12 V	2.99 A	93.21%	37 ns	43 ns
12 V	2.50 A	93.11%	34 ns	37.9 ns
12 V	2.01 A	92.44%	34 ns	33.5 ns
12 V	1.50 A	91.17%	30 ns	31 ns
12 V	1.02 A	88.21%	29 ns	28.8 ns

Figure 2.31 implies that the optimal SR turn-off delay consists of two parts: S_1 deadtime and another interval that i_{Lr} takes to reach i_{Lf}, denoted as Δt here. Since S_1 deadtime is usually a fixed one, only Δt needs to be calculated. It is assumed that

$$\Delta t = \frac{L_r \cdot (I_{out} - \frac{\Delta I}{2})}{V_{in}} \cdot K \tag{2.42}$$

where K is a proportional gain. Then the optimal SR turn-off delay is

$$t_{opt\_SR\_delay} = t_{d\_S_1} + \frac{L_r \cdot (I_{out} - \frac{\Delta I}{2})}{V_{in}} \cdot K \tag{2.43}$$

where $t_{d\_S_1}$ is the deadtime between S_2 turn-off and S_1 turn-on. This method of obtaining an optimal SR turn-off delay involves very simple calculation based on

Table 2.7: Measured Optimized SR Turn-off Delay Time at 8 V input

V_{in}	I_o	Measured Efficiency	Measured Optimal SR Turn-off Delay	Calculated Optimal SR Turn-off Delay
8 V	4.45 A	93.39%	79.9 ns	84.7 ns
8 V	3.98 A	93.53%	70.0 ns	76.5 ns
8 V	3.48 A	93.63%	61.3 ns	67.7 ns
8 V	3.03 A	93.71%	52.8 ns	59.4 ns
8 V	2.50 A	93.66%	47.3 ns	51.5 ns
8 V	1.98 A	93.37%	40.2 ns	42.4 ns
8 V	1.48 A	92.48%	35.0 ns	35.6 ns
8 V	1.06 A	90.77%	29.0 ns	30.8 ns

sensed parameters (I_{out}, V_{in}) and fixed design values (L_r, K). Therefore, it is able to do this calculation by digital control or analog circuitry during the operation of the converter and apply this turn-off delay to SR gate.

If K equals to one, it implies that, by the end of S_1 deadtime, the resonant inductor current i_{Lr} is zero. In fact, by the end of S_1 deadtime, i_{Lr} is either negative (at high load) or positive (at light load). Thus it is desired to have a larger K (>1) for calculation at high load and a smaller K (<1) for calculation at light load. At light load, since Δt is only a small part of the total SR turn-off delay time (much of the total turn-off delay time is S_1 deadtime), large K will not affect the accuracy of the calculated SR turn-off delay time much at light load. For this design, the K value is designed as 1.4. Then the comparison between two calculation algorithms is shown in Table 2.9. It is shown that the calculation results from two methods are

Table 2.8: Measured Optimized SR Turn-off Delay Time at 16 V input

V_{in}	I_o	Measured Efficiency	Measured Optimal SR Turn-off Delay	Calculated Optimal SR Turn-off Delay
16 V	4.93 A	92.60%	44 ns	50.6 ns
16 V	4.49 A	92.62%	41.6 ns	47.6 ns
16 V	4.01 A	92.72%	37.8 ns	43.2 ns
16 V	3.48 A	92.62%	34.6 ns	39.2 ns
16 V	3.23 A	92.61%	31.7 ns	37.5 ns
16 V	2.35 A	91.68%	29.5 ns	32.3 ns
16 V	1.54 A	89.10%	28.5 ns	28.4 ns
16 V	1.07 A	85.08%	27.6 ns	26.2 ns

close to each other.

Then, Figure 2.32 shows the efficiency curves with adaptive optimal SR turn-off delay at 2.2 MHz. Figure 2.33 shows the efficiency comparison of the GaN based prototype between using SR turn-off delay and not using SR turn-off delay, at 12 V input. It could be seen that the adaptive SR turn-off delay significantly improves the efficiency of the proposed active-clamp buck converter. With optimal SR turn-off delay, the peak total efficiency (including driver and control loss) is 93.22% and the total efficiency is above 91% with I_{out} >1.5 A.

It should be noted that, the optimal SR turn-off delay could also be used for Si based active-clamp buck converter only if the control circuit can calculate the optimal delay time for SR and apply this delay time to the gate of SR. In the prototype with Si MOSFETs, the commercial PWM controller LM5027 is used, which is not

Table 2.9: Comparison between Original and Simplified Calculation Algorithm for Optimal SR Turn-off Delay

I_o	Original at 8Vin	Simplified at 8Vin	Original at 12Vin	Simplified at 12Vin	Original at 16Vin	Simplified at 16Vin
1 A	30.86 ns	31.89 ns	26.84 ns	27.22 ns	25.41 ns	25.53 ns
2 A	43.57 ns	45.38 ns	33.58 ns	36.20 ns	30.44 ns	32.26 ns
3 A	60.06 ns	58.86 ns	43.09 ns	45.19 ns	35.50 ns	38.99 ns
4 A	77.67 ns	72.34 ns	54.10 ns	54.17 ns	43.37 ns	45.73 ns
5 A	96.15 ns	85.82 ns	65.55 ns	63.15 ns	51.65 ns	52.46 ns

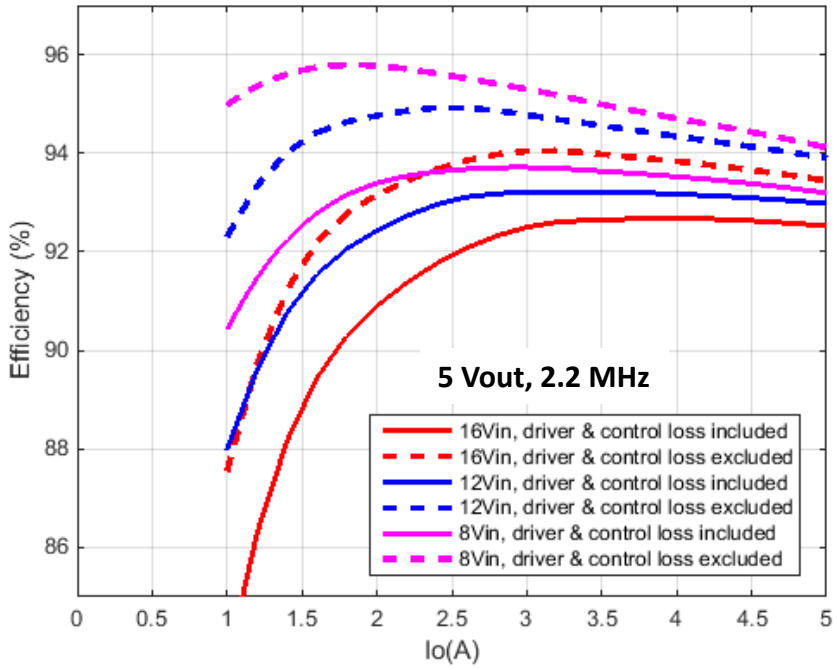


Figure 2.32: Efficiency Curves of GaN Based Active-clamp Buck Converter with Optimal SR Turn-off Delay.

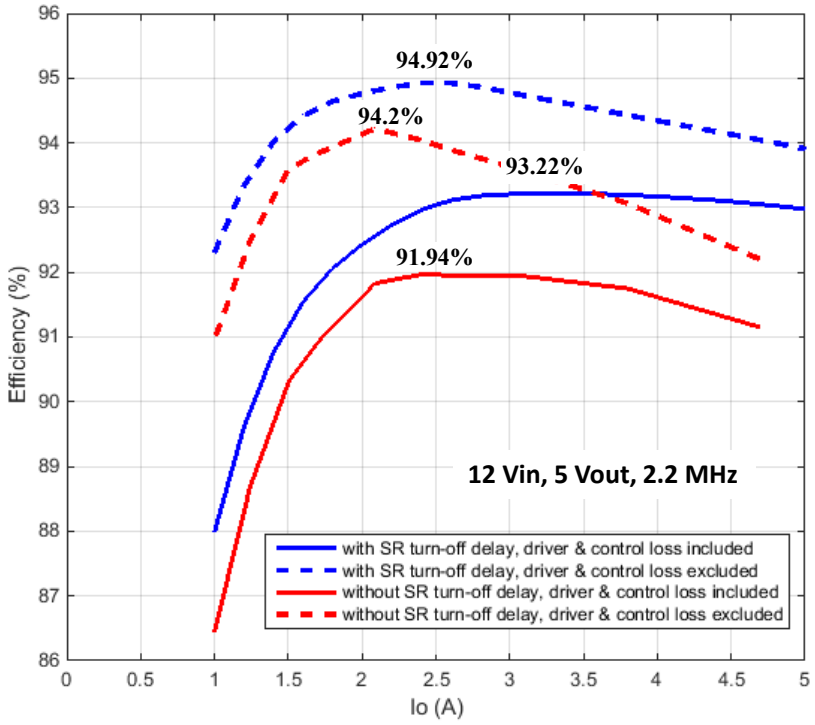


Figure 2.33: GaN Prototype Efficiency With and Without Optimal SR Turn-off Delay.

compatible with SR turn-off delay.

2.7 EMI Performance

One benefit of the proposed active-clamp buck converter is the reduced EMI noise emission due to soft-switching and slow dv/dt rate of switching. For conducted EMI, line-impedance-stabilization-network (LISN) is used for standard test. For radiated EMI, standard test requires a semi anechoic room or a TEM cell. For this project, the aim is to compare the EMI noise emission between conventional hard-switching buck and the proposed active-clamp buck converter. Therefore, for simplification, an H-field probe which is inexpensive and good for relative measurement is used to measure the EMI noise. Figure 2.34 shows the lab-made H-field probe used for the test. Figure 2.35 shows the setup for radiated EMI test. Shown on Figure 2.36 is the

Figure 2.34: Lab Made H-field Probe.

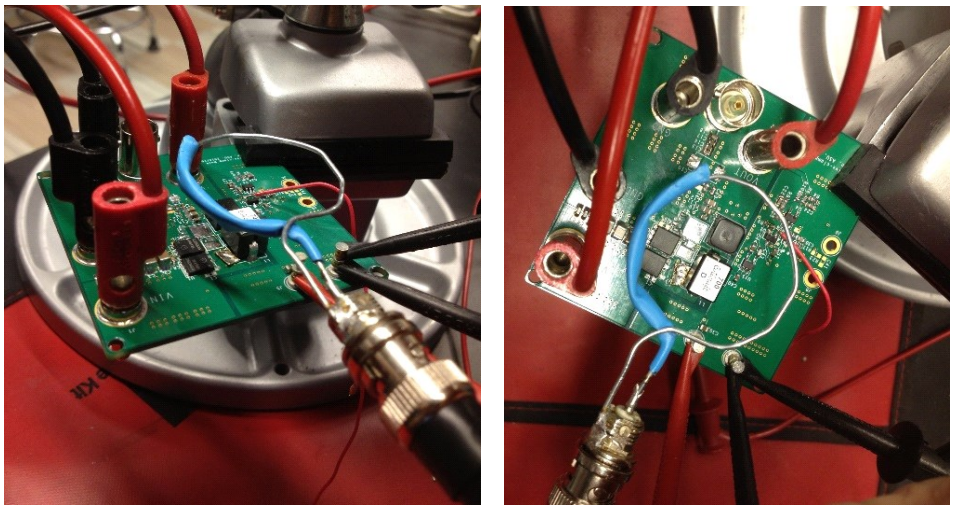


Figure 2.35: Radiated EMI Test Setup.

EMI test results for both converters running at 2.2 MHz. It is clear that the proposed active-clamp buck converter has much better EMI performance than the conventional buck converter, especially at frequencies above 20 MHz.

2.8 Modeling of the Active-clamp Buck Converter

The modeling of the proposed active-clamp buck converter is important for accurate compensator design. In this work, a straightforward and insightful averaged large-signal model for active-clamp buck converter is firstly derived, with reduced-order but high accuracy. Then, the small-signal performance is characterized and verified by Simplis simulation.

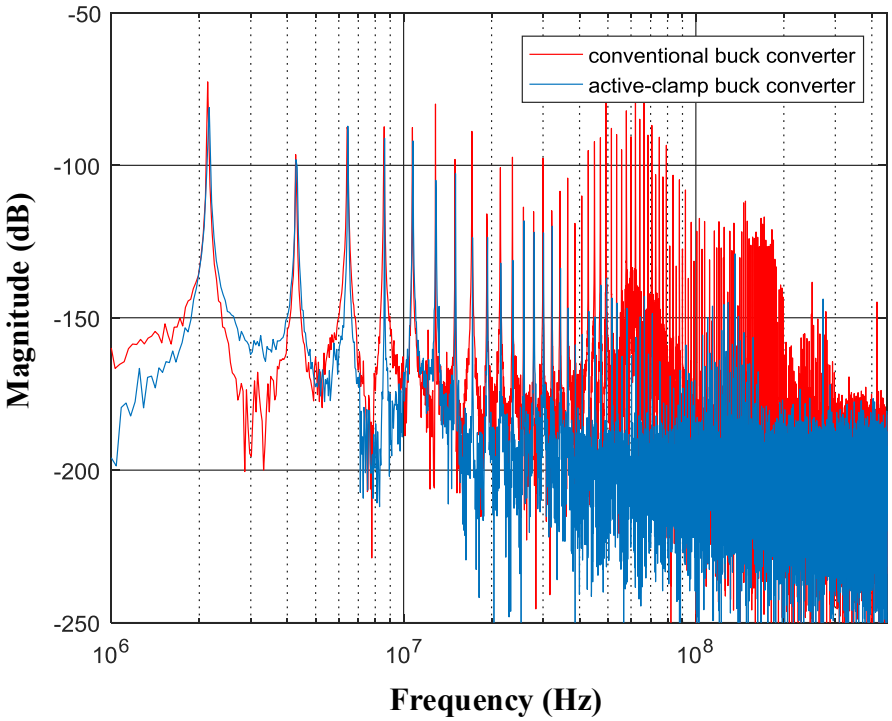


Figure 2.36: EMI Test Results for Conventional Hard-switching Buck and the Proposed Active-clamp Buck Converter.

2.8.1 Large-signal Modeling and Verification

Modeling Assumptions and Approximations

The modeling and dynamic study of the converter are of interest in the frequency range of below switching frequency or even half switching frequency. Therefore, some high frequency (higher than switching frequency) attributions of the converter are ignored during the modeling process, since they only have effects on the frequency response at very high frequency. The assumptions made here include: 1) resonant transition modes (Mode 1 and Mode 3 in 2.2) are ignored, since the intervals of these two modes are very small compared to the switching period; 2) resonance after SR body diode turn-off is ignored; 3) the circuit parasitics are not considered during the modeling. After these assumptions, the key operating waveforms are modified from

Figure 2.3 and the simplified waveforms are shown in Figure 2.37. The following model derivation is based on Figure 2.37.

Large-signal Model Derivation

Since there is one more inductor and one more capacitor in the active-clamp buck converter, compared with conventional buck converter, there are totally four state variables in this converter system: i_{Lr}, v_{clamp}, i_{Lf}, v_{Co}. Furthermore, v_{clamp}, i_{Lf}, v_{Co} are assumed to have small ripple. The model inputs include duty cycle d, input voltage v_{in} and load current i_o. The model output is v_{Co}.

As seen in Figure 2.37, there is a $\Delta d \cdot T_s$ interval indicating the duty cycle loss of the active-clamp buck converter. Therefore, the averaged voltage at the point before the output $L_f - C_o$ filter (drain node of SR) is determined by Δd, which is an intermediate variable between the state variables and the output. It is hence important to derive the expression for Δd with state variables, model inputs and circuit parameters. According to Figure 2.37, Δd is derived as

$$\Delta d = \frac{(1-d) \cdot L_f \cdot v_{clamp} - (1-d) \cdot L_r \cdot v_{Co}}{L_f \cdot v_{in} + L_r \cdot v_{C_o}} \tag{2.44}$$

Since v_{clamp}, v_{Co} and v_{in} have small ripple, Δd can also be expressed with averaged state and input variables,

$$\Delta d = \frac{(1-d) \cdot L_f \cdot \overline{v_{clamp}} - (1-d) \cdot L_r \cdot \overline{v_{Co}}}{L_f \cdot \overline{v_{in}} + L_r \cdot \overline{v_{C_o}}} \tag{2.45}$$

It is critical to notice that 2.45 is valid not only for steady state but also for transients. Then, assuming $t_1 = 0$, the state variable i_{Lr} can be expressed with Δd and other state variables and inputs,

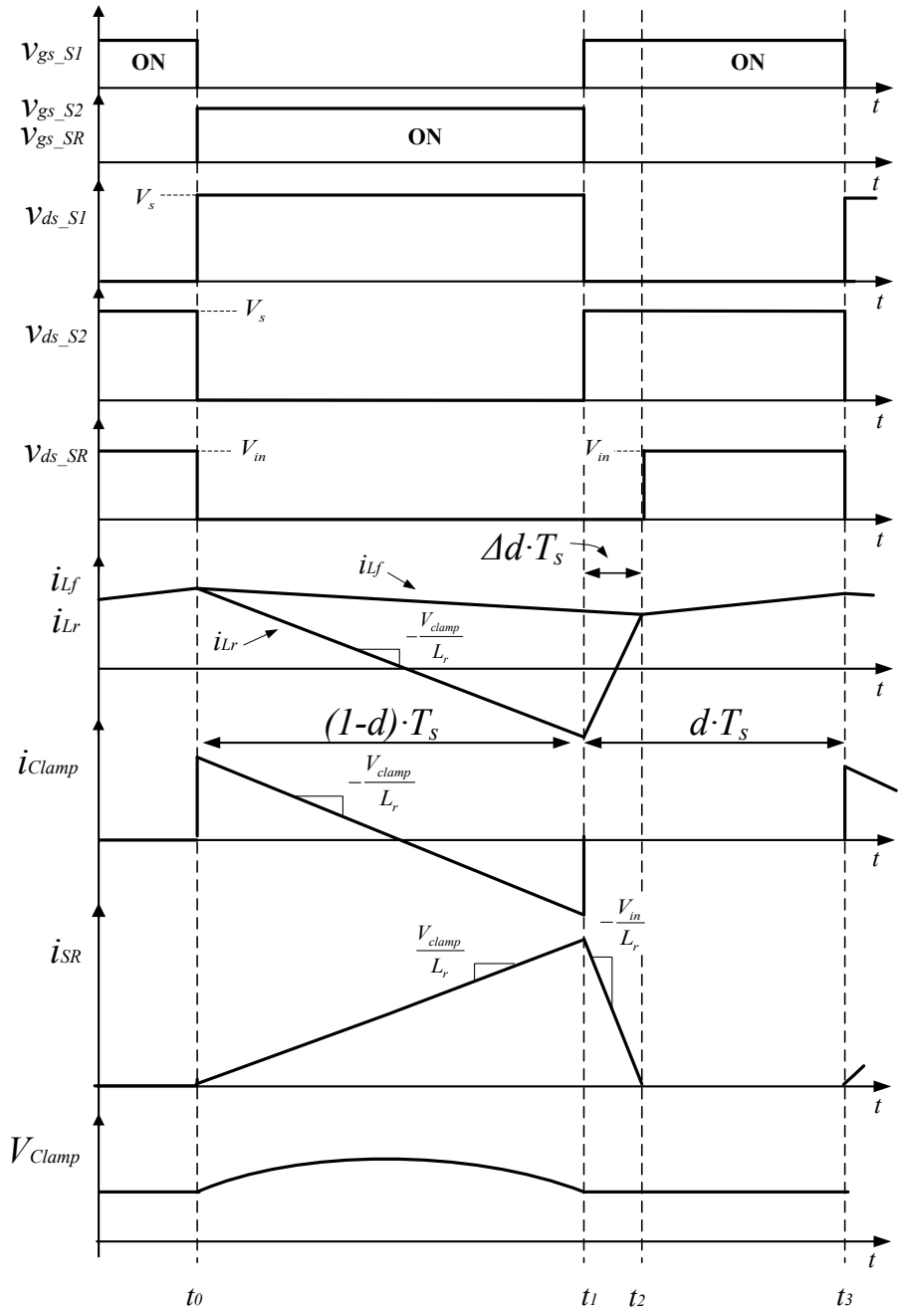


Figure 2.37: Key Operating Waveforms after Modeling Assumptions.

$$i_{Lr} = \begin{cases} i_{L_f} - \dfrac{v_{in}}{L_r} \cdot \Delta d \cdot T_s + \dfrac{v_{in}}{L_r} \cdot t & t \in [0, \Delta d \cdot T_s] \\ i_{L_f} & t \in [\Delta d \cdot T_s, d \cdot T_s] \\ i_{L_f} - \dfrac{v_{clamp}}{L_r} \cdot t & t \in [d \cdot T_s, T_s] \end{cases} \tag{2.46}$$

Since Δd is also a function of other state variables and inputs, i_{L_r} is not an independent state. Consequently, there are only three independent states: v_{clamp}, i_{L_f} and v_{Co}. Since all independent states, inputs are with small ripple, they are re-defined as

$$\boldsymbol{x} = [\overline{v_{clamp}}, \overline{i_{L_f}}, \overline{v_{Co}}]^T \tag{2.47}$$

$$\boldsymbol{u} = [d, \overline{v_{in}}, \overline{i_o}]^T \tag{2.48}$$

The state space equations for these states are

$$\frac{d\overline{v_{clamp}}}{dt} = \frac{1}{C_{clamp}} \begin{cases} 0 & t \in [0, \Delta d \cdot T_s] \\ 0 & t \in [\Delta d \cdot T_s, d \cdot T_s] \\ \overline{i_{L_r}} & t \in [d \cdot T_s, T_s] \end{cases} \tag{2.49}$$

$$\frac{d\overline{i_{L_f}}}{dt} = \begin{cases} \frac{1}{L_f} \cdot (0 - \overline{v_{Co}}) & t \in [0, \Delta d \cdot T_s] \\ \dfrac{\overline{v_{in}} - \overline{v_{Co}}}{L_r + L_f} & t \in [\Delta d \cdot T_s, d \cdot T_s] \\ \frac{1}{L_f} \cdot (0 - \overline{v_{Co}}) & t \in [d \cdot T_s, T_s] \end{cases} \tag{2.50}$$

$$\frac{d\overline{v_{Co}}}{dt} = \frac{1}{C_o} \cdot (\overline{i_{L_f}} - \frac{\overline{v_{Co}}}{R}) \tag{2.51}$$

Then, the large-signal model can be derived by averaging 2.49, 2.50 and 2.51. However, it should be noted that i_{L_r} in 2.46 is a variable with large ripple which cannot be averaged directly. From the operating principle analysis in Section 2.2, it

is found that i_{L_r} only interact with v_{clamp} when $t \in [d \cdot T_s, T_s]$, namely in $(1-d) \cdot T_s$. Thus, in 2.49, $\overline{i_{L_r}}$ should be the average value of i_{L_r} in $(1-d) \cdot T_s$, as

$$\overline{i_{L_r\text{-}(1-d)T_s}} = \overline{i_{L_f}} + \frac{\overline{v_{in}} - \overline{v_{Co}}}{2(L_r + L_f)} \cdot (d - \Delta d) \cdot T_s - \frac{\overline{v_{clamp}}}{2L_r} \cdot (1-d) \cdot T_s \tag{2.52}$$

Then, substituting 2.52 into 2.49, the averaging of the state space equations could be obtained,

$$\frac{d\overline{v_{clamp}}}{dt} = \frac{1}{C_{clamp}} \cdot [\overline{i_{L_f}} + \frac{\overline{v_{in}} - \overline{v_{Co}}}{2(L_r + L_f)} \cdot (d - \Delta d) \cdot T_s - \frac{\overline{v_{clamp}}}{2L_r} \cdot (1-d) \cdot T_s] \cdot (1-d) \tag{2.53}$$

$$\frac{d\overline{i_{L_f}}}{dt} = -\frac{\overline{v_{Co}}}{L_f} \cdot (1 - d + \Delta d) + \frac{\overline{v_{in}} - \overline{v_{Co}}}{L_r + L_f} \cdot (d - \Delta d) \tag{2.54}$$

$$\frac{d\overline{v_{Co}}}{dt} = \frac{1}{C_o} \cdot (\overline{i_{L_f}} - \frac{\overline{v_{Co}}}{R}) \tag{2.55}$$

where

$$\Delta d = \frac{(1-d) \cdot L_f \cdot \overline{v_{clamp}} - (1-d) \cdot L_r \cdot \overline{v_{Co}}}{L_f \cdot \overline{v_{in}} + L_r \cdot \overline{v_{C_o}}} \tag{2.56}$$

as derived in 2.45. 2.53 - 2.55 is thus the large-signal model of the proposed active-clamp buck converter. In order to verify the accuracy, the model is built in PLECS in comparison with a switch model, as shown in Figure 2.38. Figure 2.39 shows the simulation results when duty cycle changes from 0.8 to 0.9. It could be seen the average model results match very well with switch model results.

2.8.2 Small-signal Characterization

Based on the large-signal averaged model, defining

$$f(\boldsymbol{x}, \boldsymbol{u}) = \frac{d\boldsymbol{x}}{dt} \tag{2.57}$$

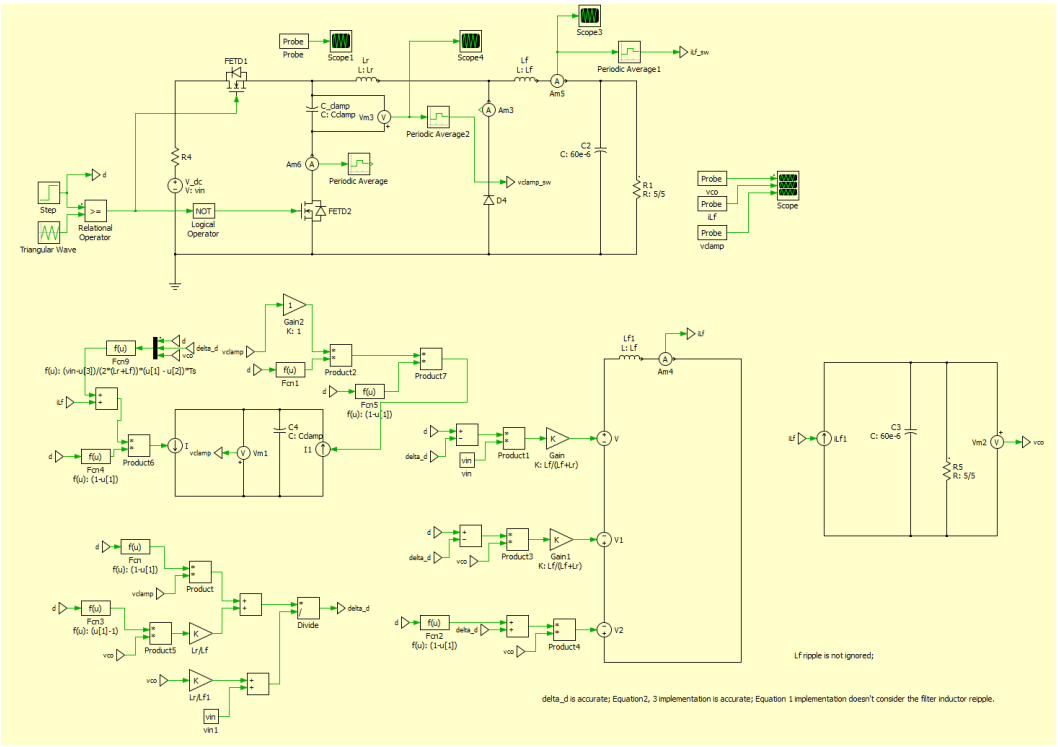


Figure 2.38: Verification of the Derived Large-signal Model.

$$g(\boldsymbol{x}, \boldsymbol{u}) = \boldsymbol{y} = [\overline{v_{Co}}]^T \tag{2.58}$$

and then $\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{C}$, $\boldsymbol{D}$ matrices could be calculated as,

$$\boldsymbol{A} = \frac{\partial f}{\partial \boldsymbol{x}}, \quad \boldsymbol{B} = \frac{\partial f}{\partial \boldsymbol{u}}, \quad \boldsymbol{C} = \frac{\partial g}{\partial \boldsymbol{x}}, \quad \boldsymbol{D} = \frac{\partial g}{\partial \boldsymbol{u}} \tag{2.59}$$

Therefore, the linearized small-signal model could be obtained,

$$\frac{d\hat{\boldsymbol{x}}}{dt} = \boldsymbol{A}\hat{\boldsymbol{x}} + \boldsymbol{B}\hat{\boldsymbol{u}} \tag{2.60}$$

$$\hat{\boldsymbol{y}} = \boldsymbol{C}\hat{\boldsymbol{x}} + \boldsymbol{D}\hat{\boldsymbol{u}} \tag{2.61}$$

and the transfer functions are also derived,

$$\boldsymbol{y}(s) = [\boldsymbol{C}(s\boldsymbol{I} - \boldsymbol{A})^{-1}\boldsymbol{B} + \boldsymbol{D}]\boldsymbol{u}(s) \tag{2.62}$$

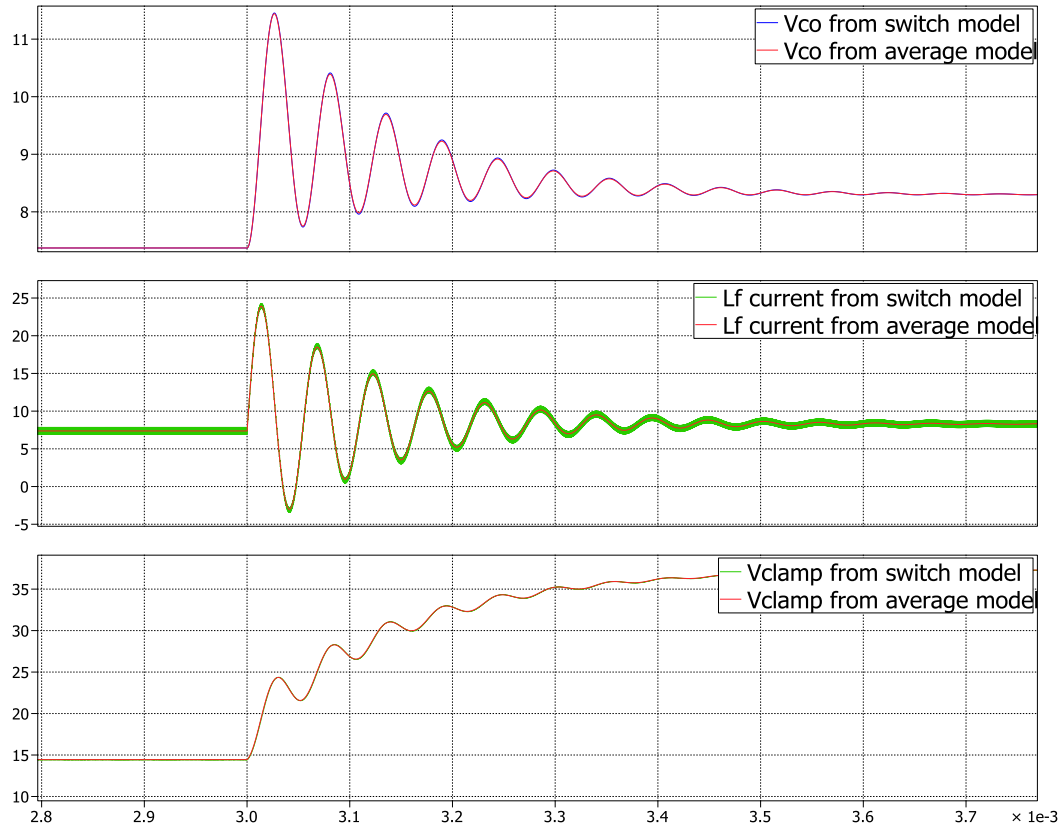


Figure 2.39: Simulation Results with Average Model and Switch Model.

Figure 2.40 shows the bode plots of control-to-output ($\hat{d}$ to $\widehat{v_{Co}}$) transfer function from Simplis simulation and the derived small-signal model. The simulation and model parameters are shown in Table 2.10. It could be seen that the magnitude plot from the model matches Simplis simulation result very well up to the half switching frequency. For the phase plot, the matching between Simplis simulation and derived model is also good till one tenth of the switching frequency. In addition, the maximum phase error between the model and simulation is only 15 °, at half switching frequency.

2.9 Summary

In this chapter, a new active-clamp buck topology is proposed for 2.2 MHz, 25 W automotive POL converters. The detailed operating principle for the circuit including

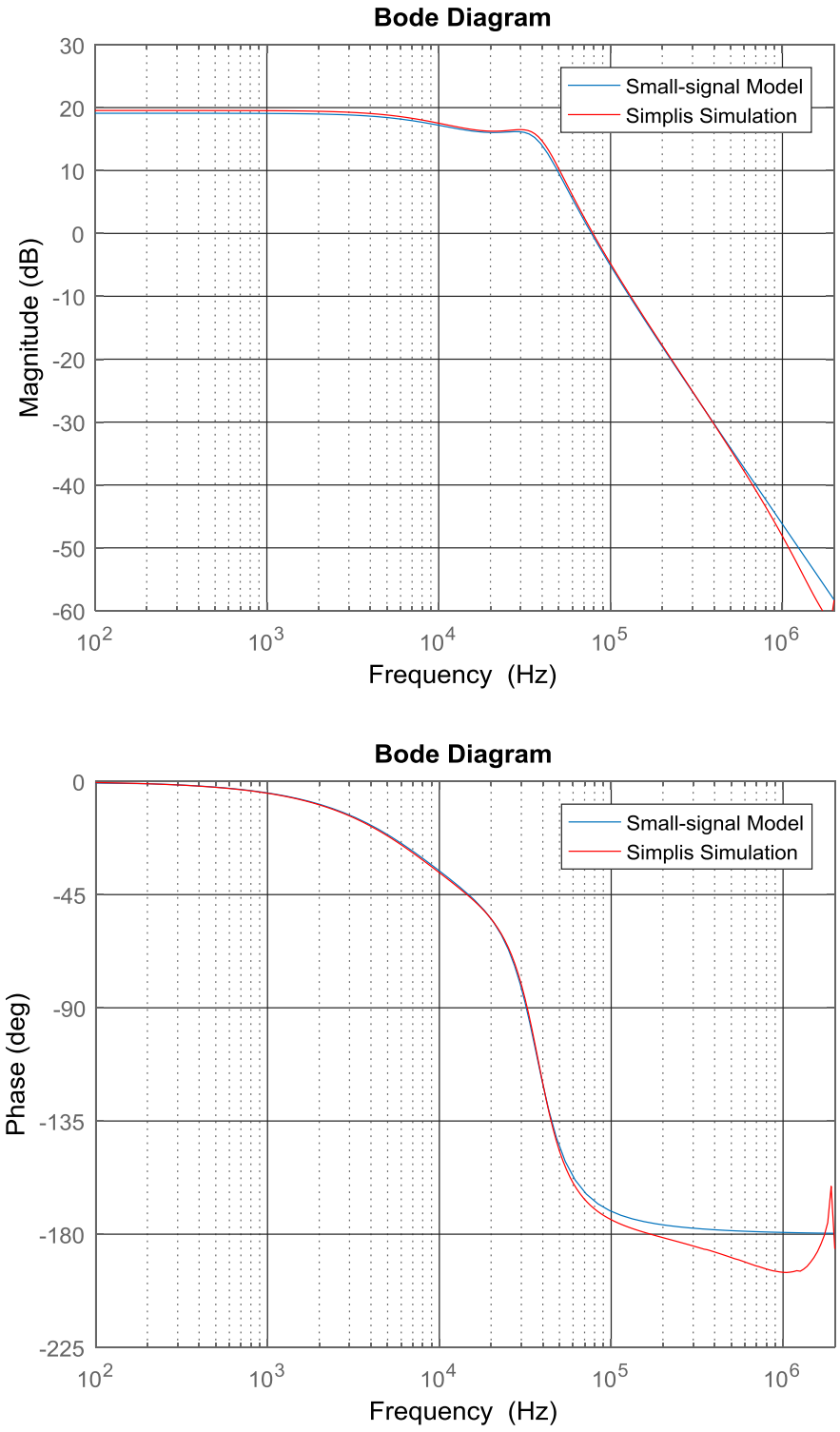


Figure 2.40: Bode Plots of the Control-to-output Transfer Function from Simplis Simulation and the Derived Small-signal Model.

Table 2.10: Simulation and Model Parameters

V_{in}	12 V
V_{out}	12 V
I_o	5 A
L_r	80 nH
L_f	1.3 uH
C_{clamp}	3 uF
C_o	60 uF
f_s	2.2 MHz

all the parasitic capacitances is presented. In addition, several important design considerations including factors affecting ZVS performance, selection of clamp capacitor and the impact of loss of effective duty cycle are addressed, leading to extensive design equations for various components. The design, implementation and evaluation of a 2.2 MHz, 5V/5A hardware prototype using only commercial silicon devices are presented in detail. The experimental results verify the converter operation, ZVS characteristics and show the limited dv/dt rate of the switching. The measured efficiency data at various operating conditions confirm the superior efficiency performance of the proposed active-clamp buck converter over the conventional buck converter. The peak efficiencies of the active-clamp buck converter can reach 89.7% and 93.5%, with and without considering the driver loss, respectively. Details of loss breakdown are presented and correlated with measured efficiency. In order to further improve the efficiency, a GaN FETs based prototype is built and tested. Also, the optimal SR turn-off delay is derived and applied to optimize the efficiency. The final efficiency

with GaN FETs and optimal SR turn-off delay reaches 93.22% at 12 V input, 5 V output and 2.2 MHz frequency. In addition, the EMI test results show significant improvement in the EMI performance with the proposed active-clamp buck converter. In the last of this chapter, the modeling of the proposed active-clamp buck converter is addressed. The large-signal averaged model and small-signal model are derived and verified with simulation, respectively. It shows that the response in the derived models matches very well to the response in the simulation with switching circuit model.

Chapter 3

BIDIRECTIONAL ZERO-VOLTAGE-TRANSITION CONVERTER WITH COUPLED-INDUCTOR FOR AUTOMOTIVE 48V/14V DUAL VOLTAGE SYSTEM

3.1 Introduction

In this chapter, a new bidirectional zero-voltage-transition (ZVT) converter with coupled-inductor is proposed for automotive 48V/14V dual voltage system [58]. The circuit diagram of the proposed converter is shown in Figure 3.1. The converter consists of two main switches S_1 and S_2, two auxiliary switches S_{aux1} and S_{aux2}, and a coupled-inductor. For high frequency applications, all switches are implemented with MOSFETs and thus there is a body-diode anti-paralleled with each switch. The coupled-inductor integrates the filter inductor and an extra winding into one magnetic structure. The primary to the auxiliary side turns ratio is 1:n. C_r is the resonant capacitor which combines external C_{ds} and output capacitance of the main switches (S_1 and S_2).

The coupled-inductor in the circuit can be modeled as a combination of a magnetizing inductance, an idea transformer with a turns ratio of $1 : n$, and a leakage inductance. The magnetizing inductance L_f, referred to the primary side, is employed as the filter inductance of the converter. L_l is the leakage inductance referred to the auxiliary side, used as the resonant inductance during the operation. The equivalent circuit is shown in Figure 3.2.

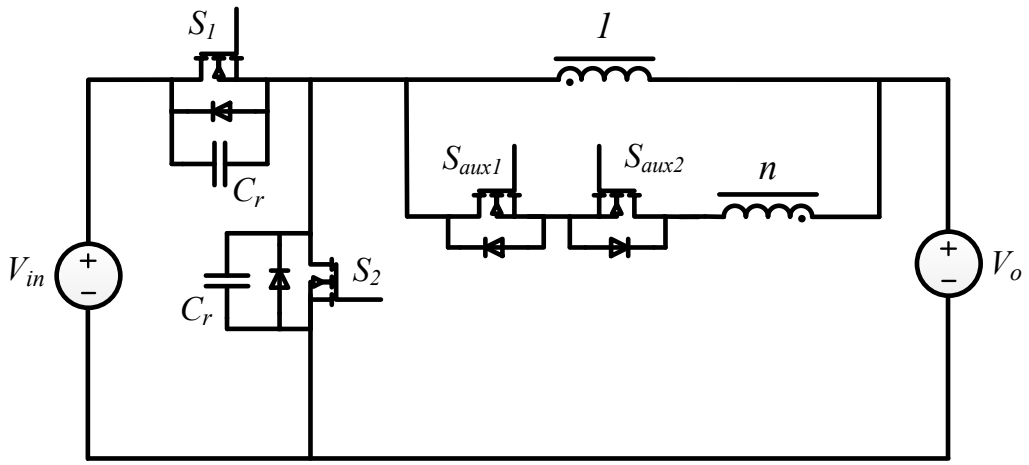


Figure 3.1: Circuit Diagram of the Proposed ZVT Converter with Coupled-inductor.

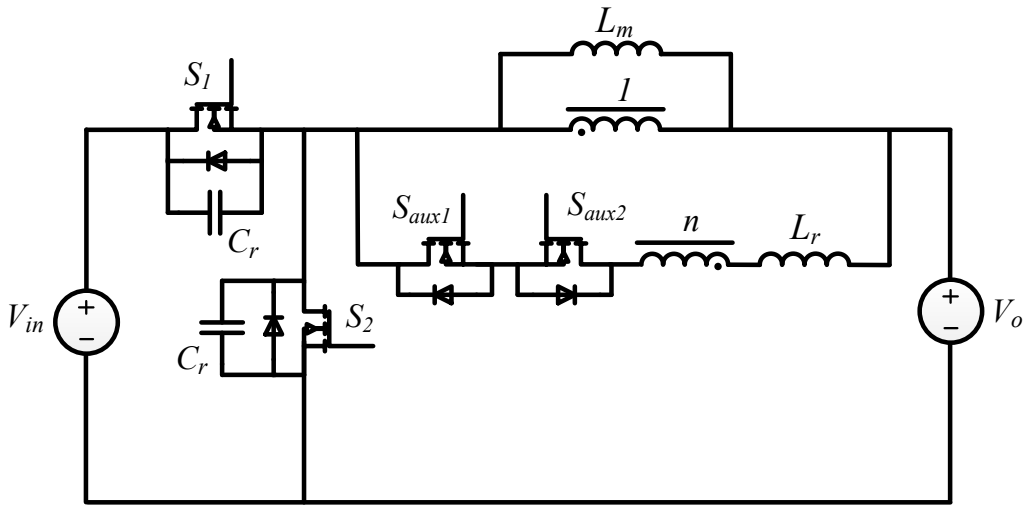


Figure 3.2: Equivalent Circuit of the Proposed ZVT Converter with Coupled-inductor.

3.2 Operating Principle Analysis

In order to simplify the analysis of operating principle, the magnetizing inductance is assumed sufficiently large so that it could be considered as a constant current source I_L. It is also assumed that all components are ideal and the circuit is operating under steady-state condition. The simplified circuit for operation analysis is shown in Figure 3.3. Figure 3.4 and 3.5 shows the key waveforms of the proposed converter in buck mode and boost mode, respectively. The reference direction for currents is indicated

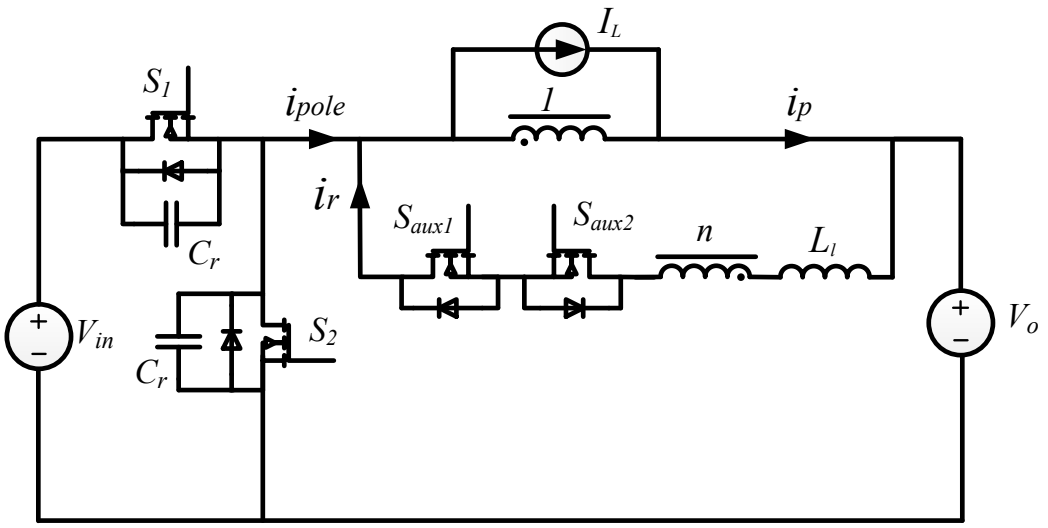


Figure 3.3: Simplified Circuit Diagram for Operating Principle Analysis.

by the arrows in Figure 3.3. It should be noted that, in the key waveforms of boost mode, the high voltage output side is still labeled as V_{in} and the low voltage input side is labeled as V_o. Since the operations of buck and boost modes are dual, only buck mode operating principle is described as following. In steady state operation, a switching cycle could be divided into eight modes and Figure 3.6 shows the topological state in each mode of buck operation.

Mode 1 $(t_8 - t_1)$

Prior to t_1, high side switch S_1 is off and low side switch S_2 (synchronous rectifier in buck mode) is conducting the magnetizing current I_L. S_{aux2} is off blocking a voltage of $(n+1) \cdot V_o$. S_{aux1} is off as well but blocks zero voltage. Thus, the auxiliary cell is off and hence no current is in the ideal transformer.

Mode 2 $(t_1 - t_2)$

At t_1, the auxiliary switch S_{aux2} turns on and then the leakage inductance L_l is linearly charged by $(n+1) \cdot V_o$ through S_{aux2}, S_{aux1} body-diode and S_2. The current

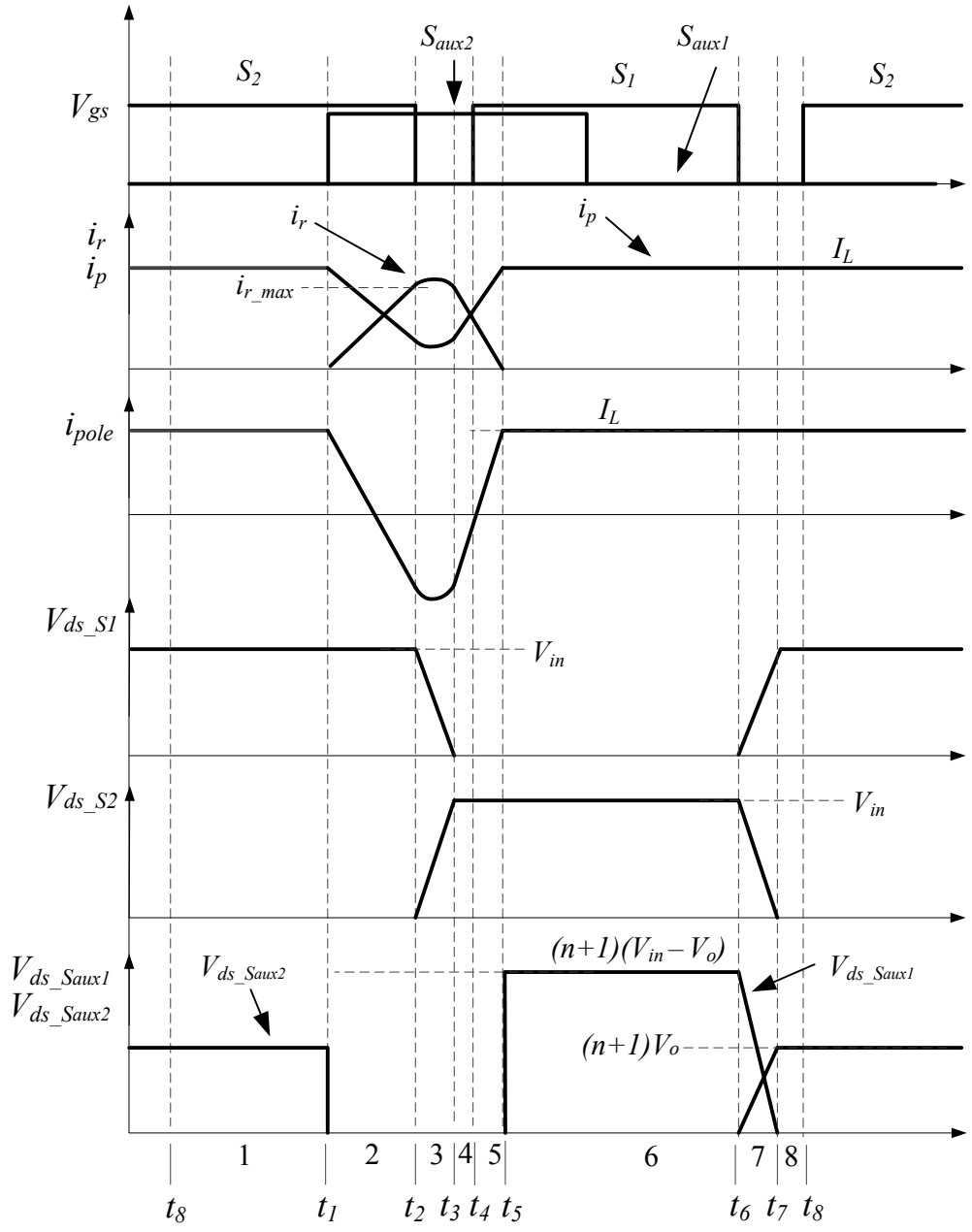


Figure 3.4: Key Operating Waveforms in Buck Mode.

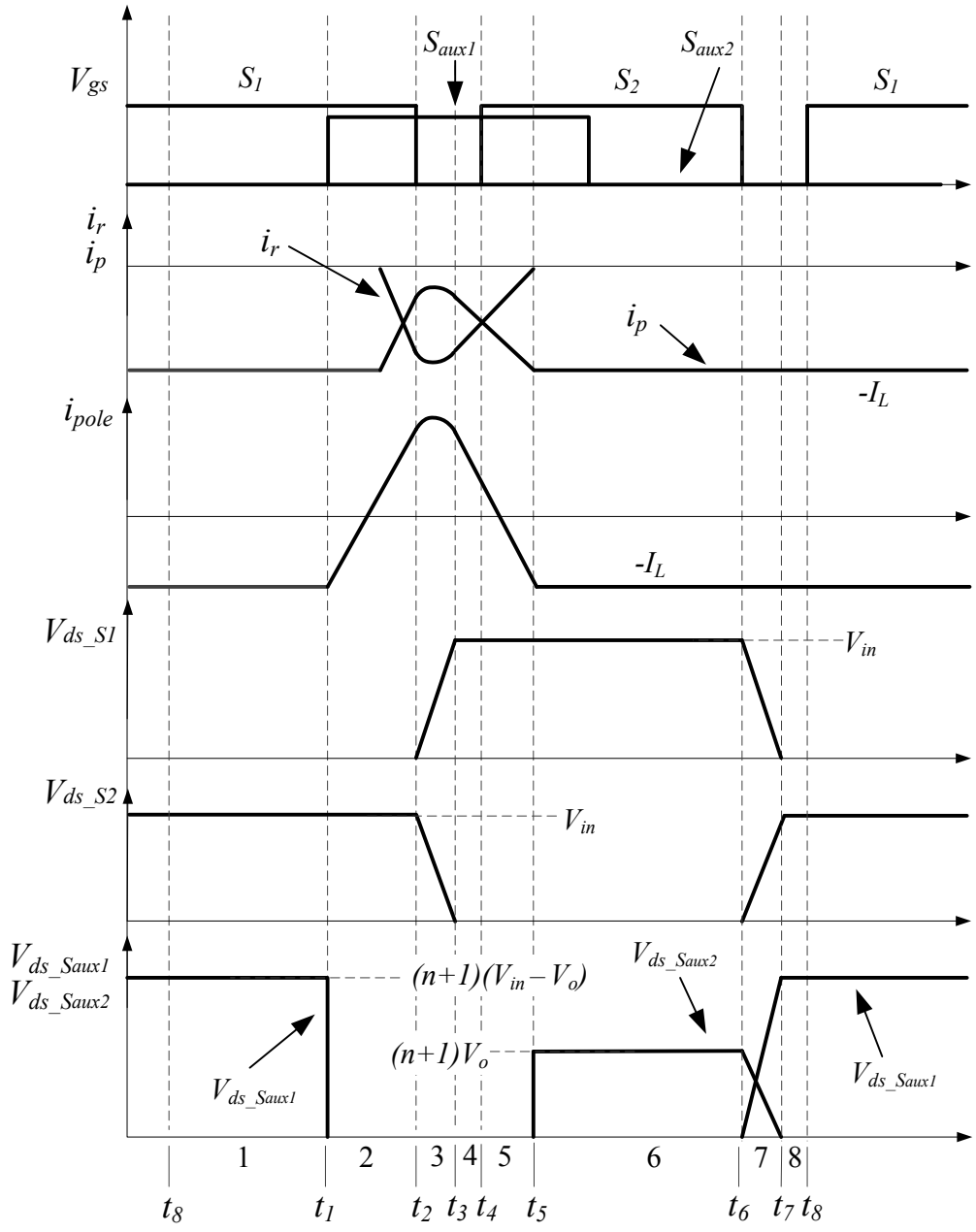


Figure 3.5: Key Operating Waveforms in Boost Mode.

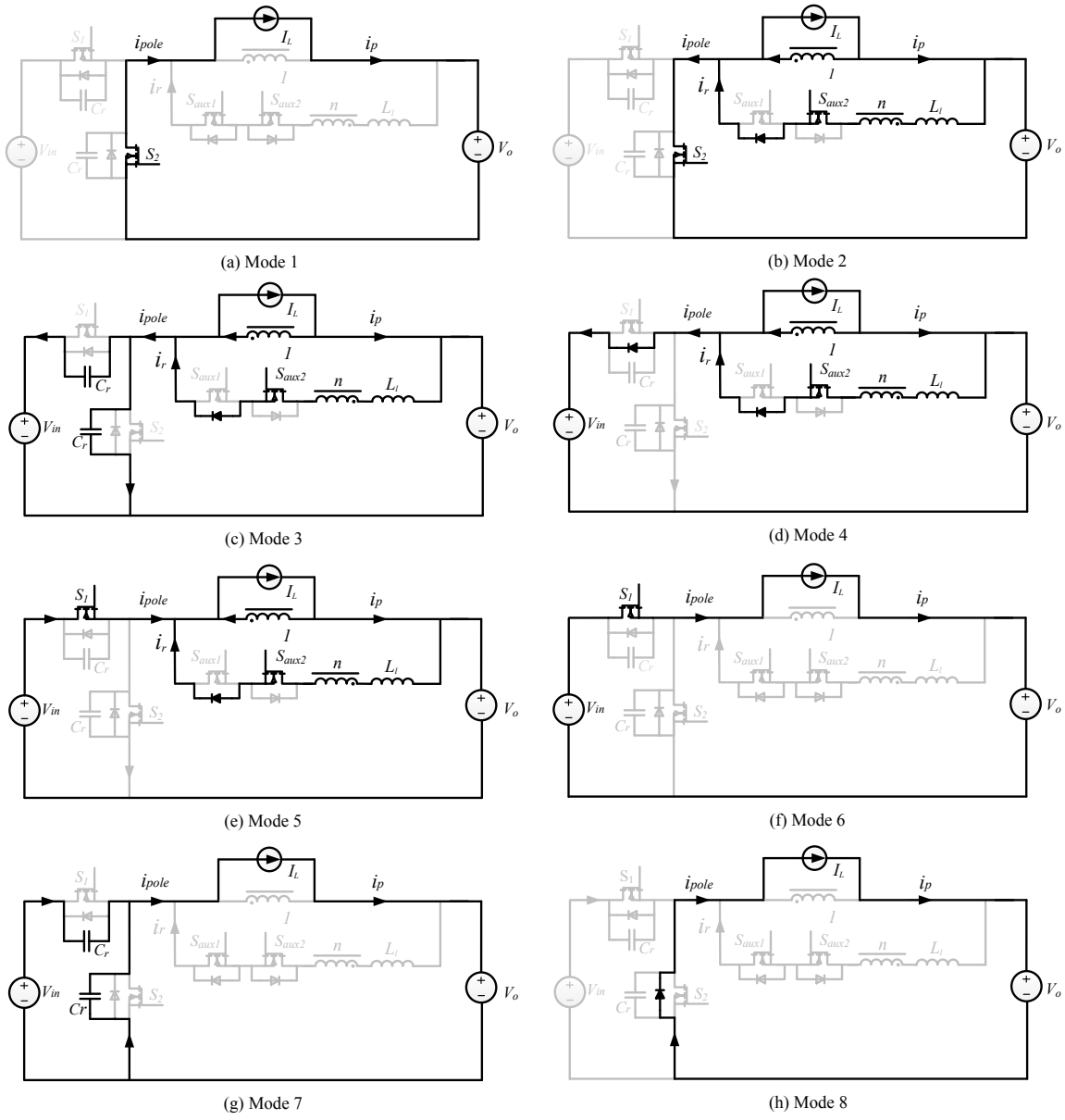


Figure 3.6: Topological State in Each Mode of Buck Operation.

in the auxiliary cell is

$$i_r = \frac{(n+1)\cdot V_o}{L_l}\cdot(t-t_1) \tag{3.1}$$

Meanwhile, due to the reverse coupling, the current in primary winding decreases proportionally,

$$i_p = I_L - n\cdot\frac{(n+1)\cdot V_o}{L_l}\cdot(t-t_1) \tag{3.2}$$

During this mode, the switching pole current i_{pole} is

$$i_{pole} = i_p - i_r = I_L - \frac{(n+1)^2\cdot V_o}{L_l}\cdot(t-t_1) \tag{3.3}$$

By the end of this mode, i_{pole} changes from positive to a negative value that is sufficient for realizing ZVS turn-on of S_1. Also, the duration of this mode is

$$t_2 - t_1 = \frac{i_{r\_max}\cdot L_l}{(n+1)\cdot V_o} \tag{3.4}$$

where i_{r_max} is a designed current value in the auxiliary cell corresponding to the sufficient i_{pole} value for ZVS.

Mode 3 ($t_2 - t_3$)

At t_2, S_2 is turned off, then i_{pole} is divided into two parts, charging and discharging the C_r of S_1 and S_2, respectively, in a resonant manner. Till t_3, the voltages across S_2 and S_1 reach V_{in} and zero, respectively. The resonant currents in the auxiliary cell during this mode is derived as

$$i_r = \frac{V_o\cdot sin[(n+1)\cdot\omega(t-t_2)]}{Z} + \frac{I_L}{n+1}\cdot(1-cos[(n+1)\cdot\omega(t-t_2)]) + i_{r\_max}\cdot cos[(n+1)\cdot\omega(t-t_2)] \tag{3.5}$$

Then, i_{pole} is

$$i_{pole} = I_L - \frac{(n+1)\cdot V_o \cdot sin[(n+1)\cdot\omega(t-t_2)]}{Z} - I_L \cdot (1 - cos[(n+1) \cdot\omega(t-t_2)]) - (n+1)\cdot i_{r\_max} \cdot cos[(n+1)\cdot\omega(t-t_2)] \quad (3.6)$$

where

$$\omega = \frac{1}{\sqrt{L_r \cdot 2C_r}}, \;\; Z = \sqrt{\frac{L_r}{2C_r}} \quad (3.7)$$

Also, the voltages across S_1 and S_2 during this mode are

$$v_{S1} = V_{in} - (i_{r\_max} - \frac{I_L}{n+1})\cdot Z \cdot sin[(n+1)\cdot\omega(t-t_2)] - V_o \cdot (1 - cos[(n+1)\cdot\omega(t-t_2)]) \quad (3.8)$$

$$v_{S2} = V_{in} - v_{S1} = (i_{r\_max} - \frac{I_L}{n+1}) \cdot Z \cdot sin[(n+1)\cdot\omega(t-t_2)] + V_o \cdot (1 - cos[(n+1)\cdot\omega(t-t_2)]) \quad (3.9)$$

Mode 4 ($t_3 - t_4$)

During this mode, the body-diode of S_1 is forward biased. L_l starts being linearly discharged by $(n+1)\cdot(V_{in} - V_o)$, and i_{pole} is still negative. S_1 should be turned on within this mode to realize ZVS.

Mode 5 ($t_4 - t_5$)

L_l continues being linearly discharged by $(n+1)\cdot(V_{in} - V_o)$ till its current i_r falls to zero, at t_5, and then the body-diode of S_{aux1} is turned off softly. Consequently, the current in the primary winding of the coupled inductor rises back to I_L. Also, i_{pole} increases back to I_L. The currents during this mode are expressed as

$$i_r = i_r(t_4) - \frac{(n+1)\cdot(V_{in} - V_o)}{L_l} \cdot (t - t_4) \quad (3.10)$$

$$i_p = I_L - n \cdot i_r = I_L - n \cdot i_r(t_4) + \frac{n \cdot (n+1) \cdot (V_{in} - V_o)}{L_l} \cdot (t - t_4) \tag{3.11}$$

$$i_{pole} = i_p - i_r = I_L - (n+1) \cdot i_r(t_4) + \frac{(n+1)^2 \cdot (V_{in} - V_o)}{L_l} \cdot (t - t_4) \tag{3.12}$$

Mode 6 $(t_5 - t_6)$

During this mode, S_{aux2} is switched off with ZCS. I_L flow from input to output through S_1. S_{aux1} is off blocking a voltage of $(n+1) \cdot (V_{in} - V_o)$.

Mode 7 $(t_6 - t_7)$

S_1 is turned off at t_6. During this mode, switching pole current is transferred from S_1 to the body-diode of S_2 in a soft-switching manner. The transition in this mode is the same as that in a conventional synchronous buck converter. Also, it should be noted that, during this transition, the voltage blocking device in the auxiliary cell is changed from S_{aux1} to S_{aux2}, and the blocked voltage is changed from $(n+1) \cdot (V_{in} - V_o)$ to $(n+1) \cdot V_o$.

Mode 8 $(t_7 - t_8)$

The body-diode of S_2 is forward biased in this mode and S_2 should be turned on within this mode to achieve ZVS. After t_8, S_1 is off and S_2 is on. Circuit state is the same as that in Mode 1.

3.3 Converter Features

From the above analysis of operating principle, it could be seen that the proposed bidirectional ZVT converter with coupled-inductor has several advantages for

automotive dual voltage system.

Soft-switching for all switches

In the proposed converter, two main switches S_1 and S_2 are switched with ZVS and auxiliary switches S_aux1 and S_aux2, and their body-diodes, are switched with ZCS. Therefore, it has potential to achieve high efficiency and low EMI noise at high frequency operation.

Wide ZVS range

In many other soft-switching converters, ZVS is lost at light load or at high input voltage. The proposed converter can still achieve ZVS at light load and at high voltage only if the i_r is sufficiently large and then the energy stored in leakage inductance would be enough to charge and discharge the resonant capacitors paralleled with S_1 and S_2, respectively. Actually, for this ZVT converter, achieving ZVS at light load is easier.

Low conduction loss in auxiliary cell

Because of the coupled-inductor, the peak current required in the auxiliary cell could be much lower than the magnetizing inductance current while the ZVS of S_1 (in buck mode) or S_2 (in boost mode) is still realized. Furthermore, with the coupled-inductor, the charging and discharging voltage across the leakage inductance during Mode 2 and Mode 4 are increased by a factor of $(n+1)$, compared to the charging and discharging voltages with a separate resonant inductor. Then the charging and discharging time is much shortened. Therefore, with the coupled-inductor, the average current and hence conduction loss in the auxiliary cell, which is a very lossy part in high current applications, could be much reduced.

Low magnetic core loss

Another benefit comes from the coupled-inductor is much reduced magnetic core loss. In the ZVT converter with a separate resonant inductor, the large current swing in the resonant inductor results in a considerable core loss, especially at high current and high frequency application. However, the coupled-inductor helps to cancel the large flux generated by the large current swing. Therefore, the core loss is only related to the current ripple in the magnetizing inductance, which is usually small. In addition, the cancellation of large flux help to reduced the winding loss caused by proximity effect.

Compact size

Compared with the filter inductor in conventional buck/boost converter, the coupled-inductor in the proposed converter only needs a secondary winding which carries a small average current. Thus secondary winding space could be small. The magnetic core size could be basically unchanged from that in a conventional buck/boost converter running at the same frequency. However, with ZVS operation, the switching frequency in the proposed ZVT converter could be much higher, resulting in smaller passive components size.

3.4 Design Considerations

3.4.1 ZVS Analysis

S_1 and S_2 work as the synchronous rectifier in boost and buck mode, respectively. The energy for achieving ZVS comes from the magnetizing inductance. Thus, it is natural to achieve ZVS for S_1 in boost mode and S_2 in buck mode.

However, for S_1 in buck mode and S_2 in boost mode, the energy to achieve ZVS

is from the energy stored in the leakage inductance. To realize ZVS for the given circuit parameters, there is a minimum current required in the leakage inductance before the switching transition. Here, the buck mode is taken as an example for calculating the minimum current requirement but the result also applies to the boost mode operation.

The targeted ZVS transition corresponds to Mode 3 in the operating principle analysis. The voltage expression of S_1 during this mode, as shown in 3.8, is repeated here.

$$v_{S1} = V_{in} - (i_{r\_max} - \frac{I_L}{n+1}) \cdot Z \cdot sin[(n+1) \cdot \omega(t-t_2)] - V_o \cdot (1 - cos[(n+1) \cdot \omega(t-t_2)]) \tag{3.13}$$

In order to achieve ZVS of S_1, the minimum value of v_{S1} in (3.13) should be less than zero. Then it could be derived that

$$i_{r\_max} \geq \sqrt{\frac{2C_r \cdot V_{in} \cdot (V_{in} - 2V_o)}{L_l}} + \frac{I_L}{n+1} \tag{3.14}$$

where i_{r_max} is the required leakage inductance current before the ZVS transition. For both buck and boost operation, the magnitude of this required leakage current is the same. Also, this is a designed value by designing the time interval by which the auxiliary cell is turned on prior to the turn-off of S_2 (in buck mode) or S_1 (in boost mode). Equation (3.14) also demonstrates how the turns ratio of the coupled-inductor affect the required peak current value (for achieving ZVS) in the auxiliary cell.

3.4.2 Auxiliary Switch Gate Timing

Auxiliary switch gate timing is critical in the proposed converter. In the buck mode S_{aux2} should turn on prior to the turn-off of S_2 by an interval of $t_2 - t_1$, as shown in Figure 3.4. Similarly, in the boost mode, S_{aux1} should turn on before the turn-off of S_1 by $t_2 - t_1$.

Considering above ZVS analysis, $t_2 - t_1$ in buck mode is calculated as

$$t_2 - t_1 \geq \frac{i_{r\_max} \cdot L_l}{(n+1) \cdot V_o} \tag{3.15}$$

For the boost mode,

$$t_2 - t_1 \geq \frac{i_{r\_max} \cdot L_l}{(n+1) \cdot (V_{in} - V_o)} \tag{3.16}$$

Also, it should be noted that the auxiliary switch should turn off after the leakage inductance current falls to zero. In buck mode,

$$t_5 - t_4 = \frac{i_r(t_3) \cdot L_l}{(n+1) \cdot (V_{in} - V_o)} \tag{3.17}$$

In boost mode,

$$t_5 - t_4 = \frac{|i_r(t_3)| \cdot L_l}{(n+1) \cdot V_o} \tag{3.18}$$

where $i_r(t_3)$ is usually assumed equal to i_{r_max} for simplifying the design. The interval $t_4 - t_2$, denoted as t_d, is the deadtime between S_1 and S_2 during which the resonant transition happens. Thus, the minimum on-time $t_{on\_minimum}$ for each auxiliary switch is

$$t_{on\_minimum} = t_5 - t_1 = \frac{i_{r\_max} \cdot L_l}{(n+1) \cdot V_o} + \frac{i_{r\_max} \cdot L_l}{(n+1) \cdot (V_{in} - V_o)} + t_d \tag{3.19}$$

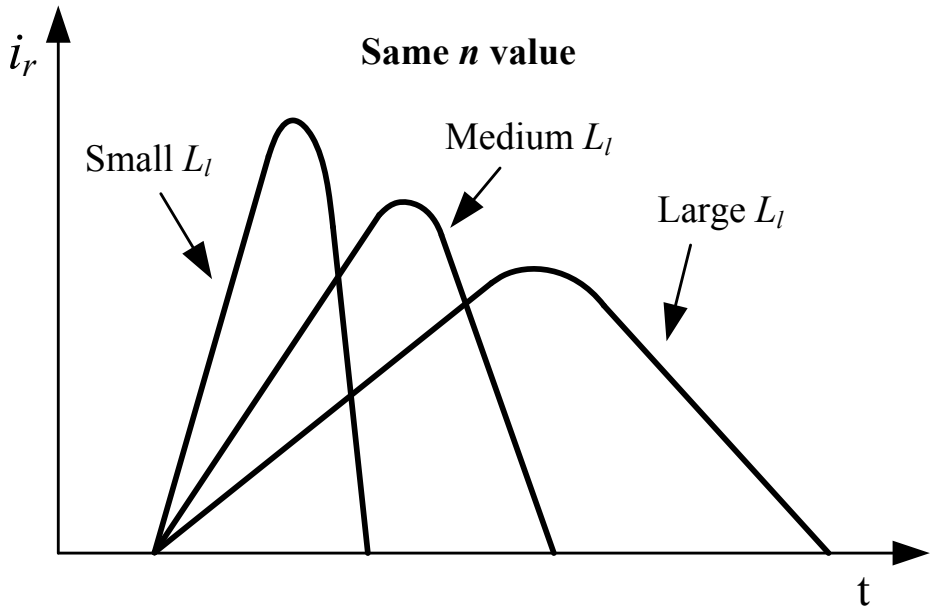


Figure 3.7: Auxiliary Cell Current with Different L_l Value.

3.4.3 Design of Leakage Inductance

The leakage inductance of the coupled-inductor is a key parameter in the proposed ZVT converter. Although any leakage inductance can store enough energy to achieve ZVS, it determines the shape of the current and hence the conduction loss in the auxiliary cell. Figure 3.7 and 3.8 show the auxiliary cell current waveforms with different leakage inductances and coupled-inductor turns ratios (n), respectively. The turns ratio of zero corresponds to the design in which a separate resonant inductor is used.

The conduction loss in the auxiliary cell consists of the body-diode forward conduction loss and the RMS current loss in resistance. It is hence related to the average and RMS currents in the cell. To eliminate the relationship with the switching period (or frequency), the average current is estimated to be proportional to the area under the current waveform, denoted as A_{i_r}. The proportional gain is value of the switching frequency. According to the operating principle analysis, the equations describing

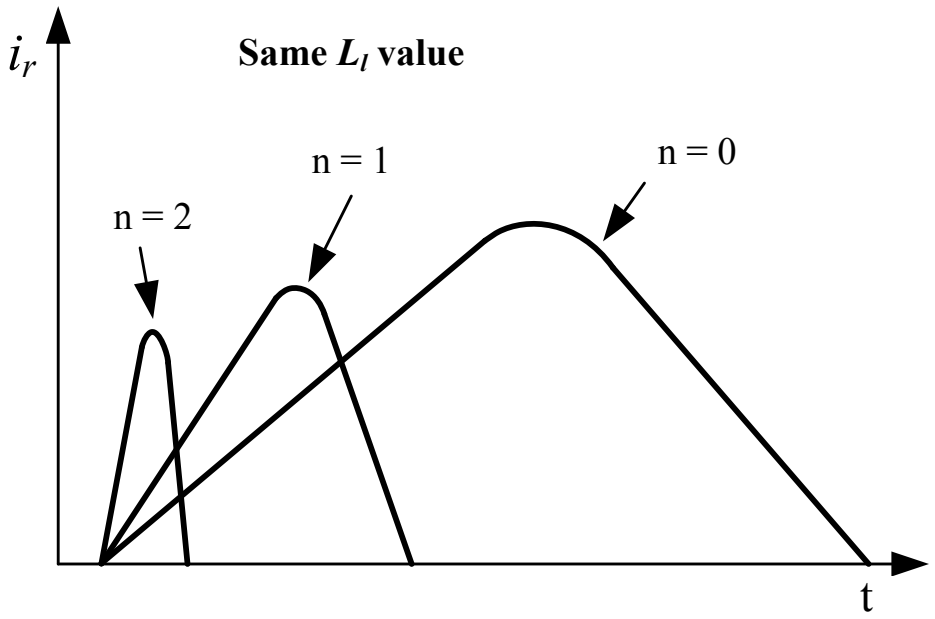


Figure 3.8: Auxiliary Cell Current with Different Coupled-inductor Turns Ratio n.

the auxiliary cell current and its duration could be derived, assuming 1) i_{r_max} is just enough to achieve ZVS; 2) deadtime is the same as the resonant transition time. Figure 3.9 shows A_{i_r} versus L_l, for a given set of parameters. It is observed that A_{i_r} decreases a lot as n changes from 0 to 1. Also, A_{i_r} decreases as L_l decreases. Thus, lower leakage inductance results in a lower value of average current in the auxiliary cell.

However, keeping decreasing L_l is not practical, and it may also increase RMS current in the auxiliary cell. Figure 3.10 shows the relationship between L_l and ampere-squared-second ($\int_{t_1}^{t_5} i_r^2 dt$) in the auxiliary cell. Interval $t_5 - t_2$ is the current duration in the auxiliary cell and $\int_{t_1}^{t_5} i_r^2 dt$ equals to $i_{r\_RMS}^2 \cdot T_s$. From Figure 3.10, it could be seen that, for each n, there is a value of L_l corresponding to the minimum ampere-squared-second and hence the minimum RMS current in the auxiliary cell. In most designs, the leakage inductance should be designed to this L_l value. It is also noticed that the coupling ($n \neq 0$) helps to reduce the ampere-squared-second and

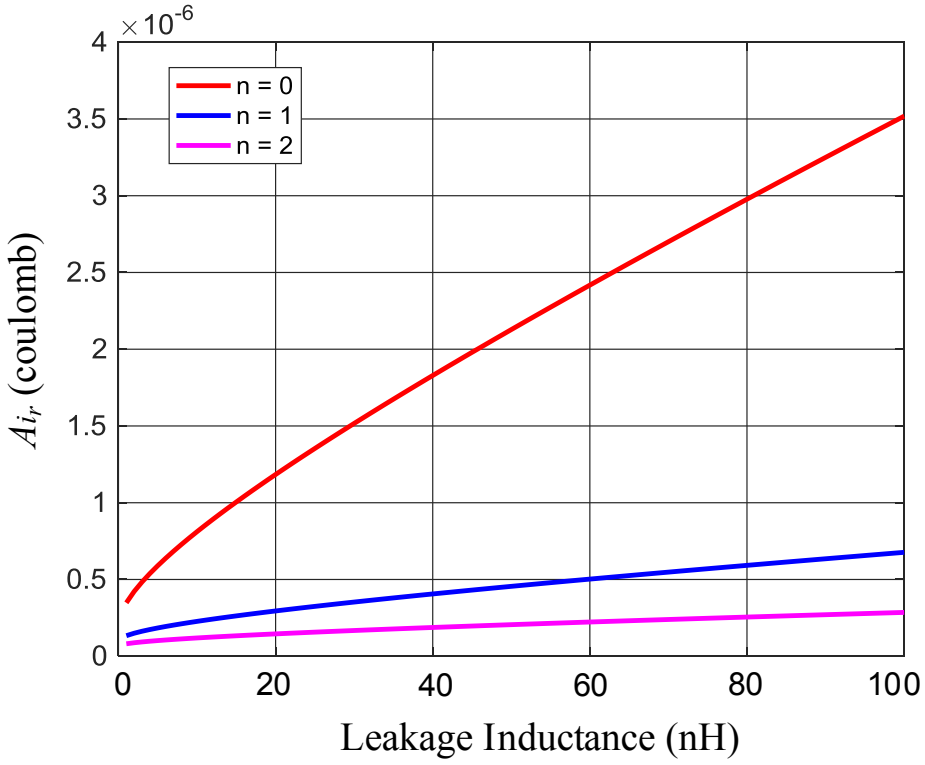


Figure 3.9: Index of Average Current in the Auxiliary Cell (A_{i_r}) at Different L_l Values.

hence the RMS current significantly.

3.4.4 Determination of Turns Ratio

The turns ratio of the coupled-inductor is another parameter needs to be designed. Higher turns ratio helps to reduce the conduction loss in the auxiliary cell but increases the voltage stress on the auxiliary switches. With a turns ratio of n, for both buck and boost modes, the voltage stresses on S_{aux1} and S_{aux2} are $(n+1)\cdot(V_{in}-V_o)$ and $(n+1)\cdot V_o$, respectively. Thus, a trade-off exists during the selection of the turns ratio.

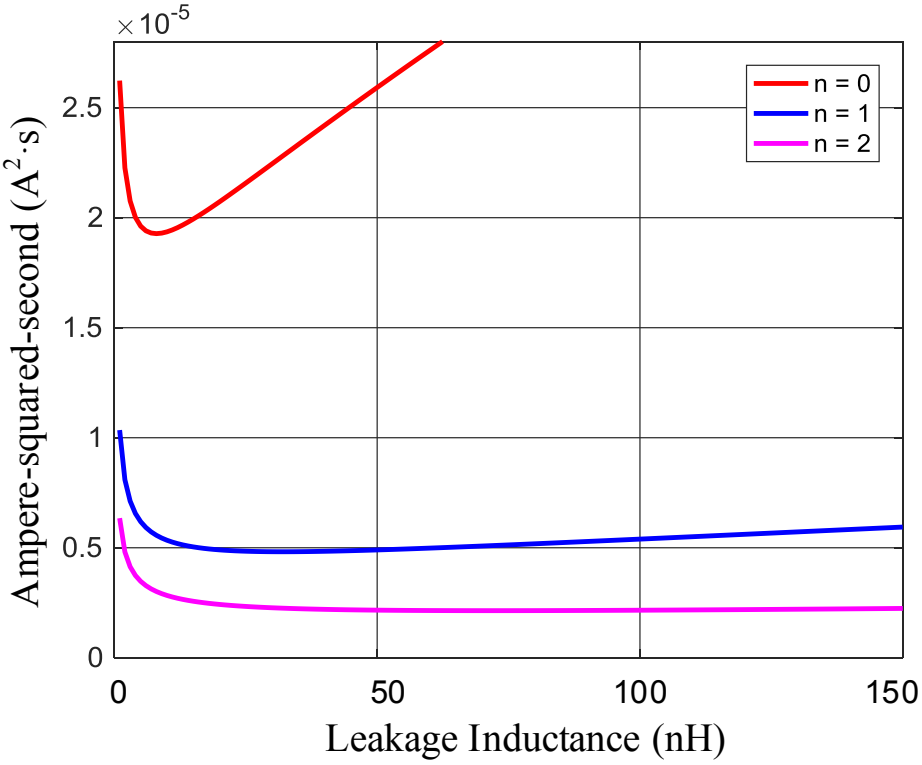


Figure 3.10: Index of RMS Current in the Auxiliary Cell (Ampere-squared-second) at Different L_l Values.

3.5 Converter Design and Simulation

3.5.1 Design Specifications

For automotive dual voltage system, power rating of the 48V/14V bidirectional converter usually ranges from 1 kW to 3 kW. For better efficiency and thermal management, interleaving is usually employed for this converter. Also, by interleaving, the converter power capability could be easily scaled up as required. However, the power capability for each phase needs to be determined. Lower power rating for each phase helps to reduce the power loss and better dissipate the heat while it requires more components and hence cost. For a compromise of thermal management and number of components, the power rating for each phase is specified as 250 W in this work. Therefore, a 250 W prototype is designed and eventually built to verify opera-

Table 3.1: Prototype Design Specifications

Rated Power	250 W
Switching Frequency	1 MHz
High Side Voltage	24 - 54 V
Low Side Voltage	10 - 16 V

tion of the proposed bidirectional ZVT converter with coupled-inductor. The design specification of the prototype is shown in Table 3.1.

3.5.2 Turns Ratio of the Coupled-Inductor

Aforementioned analysis shows that higher turns ratio n results in higher voltage rating for the auxiliary MOSFETs. It also should be noted, from Figure 3.9 and 3.10, that the average and RMS current in auxiliary cell have most significant improvement from $n = 0$ to $n = 1$; however, the improvement from $n = 1$ to $n = 2$ is not that significant. It could be proved that the marginal improvement is less and less as n increases. Therefore, a turns ratio of $1 : 1$ is designed considering the trade-off between the voltage stress and current stress on auxiliary switches.

3.5.3 Leakage Inductance of the Coupled-Inductor

It should be noted that the optimal leakage inductance determined in Section 3.4.3 varies with the operating conditions, especially the filter inductor current. Figure 3.11 shows the ampere-squared-second versus L_l with 48V/14V input/output, $1 : 1$ turns ratio and different I_L value. It could be seen that the optimal L_l value is low for high load situation while the optimal L_l value increase as load decreases. To balance the optimization at both high load and light load situations and also considering

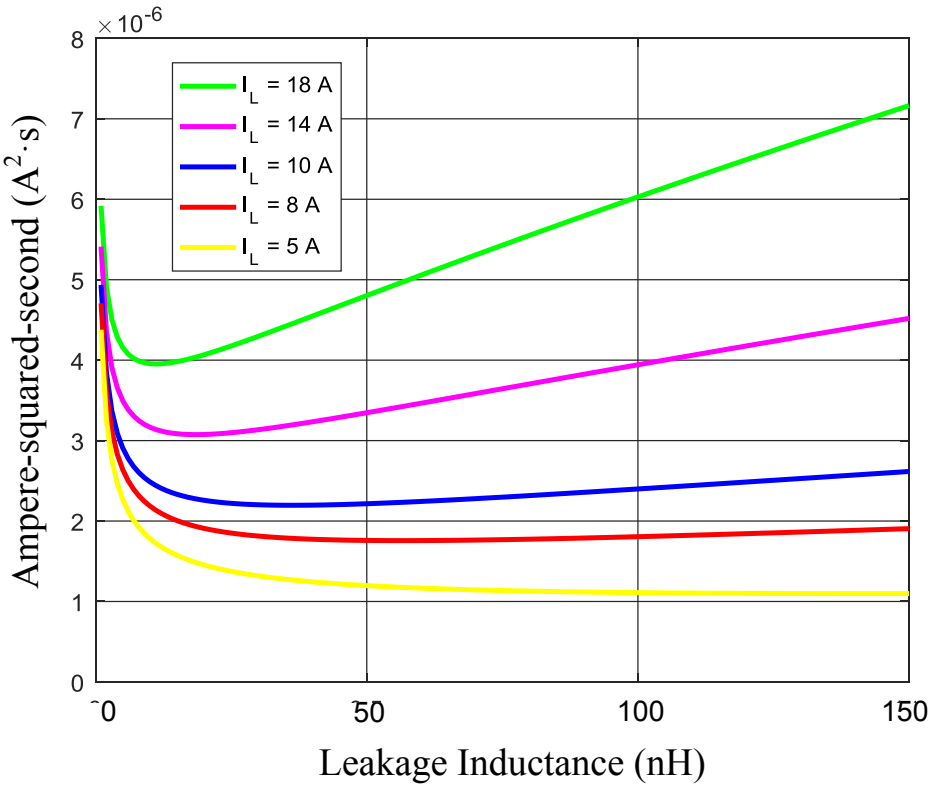


Figure 3.11: Ampere-squared-second versus L_l with 48V/14V Input/Output, 1 : 1 Turns Ratio and Different I_L Value.

the minimum leakage inductance achievable by the coupled-inductor, the leakage inductance is designed to be 40 nH.

3.5.4 Converter Simulation

Table 3.2 shows the designed parameters for the prototype and Figure 3.12 shows simulation results at 48 V input, 14 V output and 18 A load under buck operation. It can be seen that the ZVS for both S_1 and S_2 are realized even when the auxiliary branch peak current is less then the primary winding current.

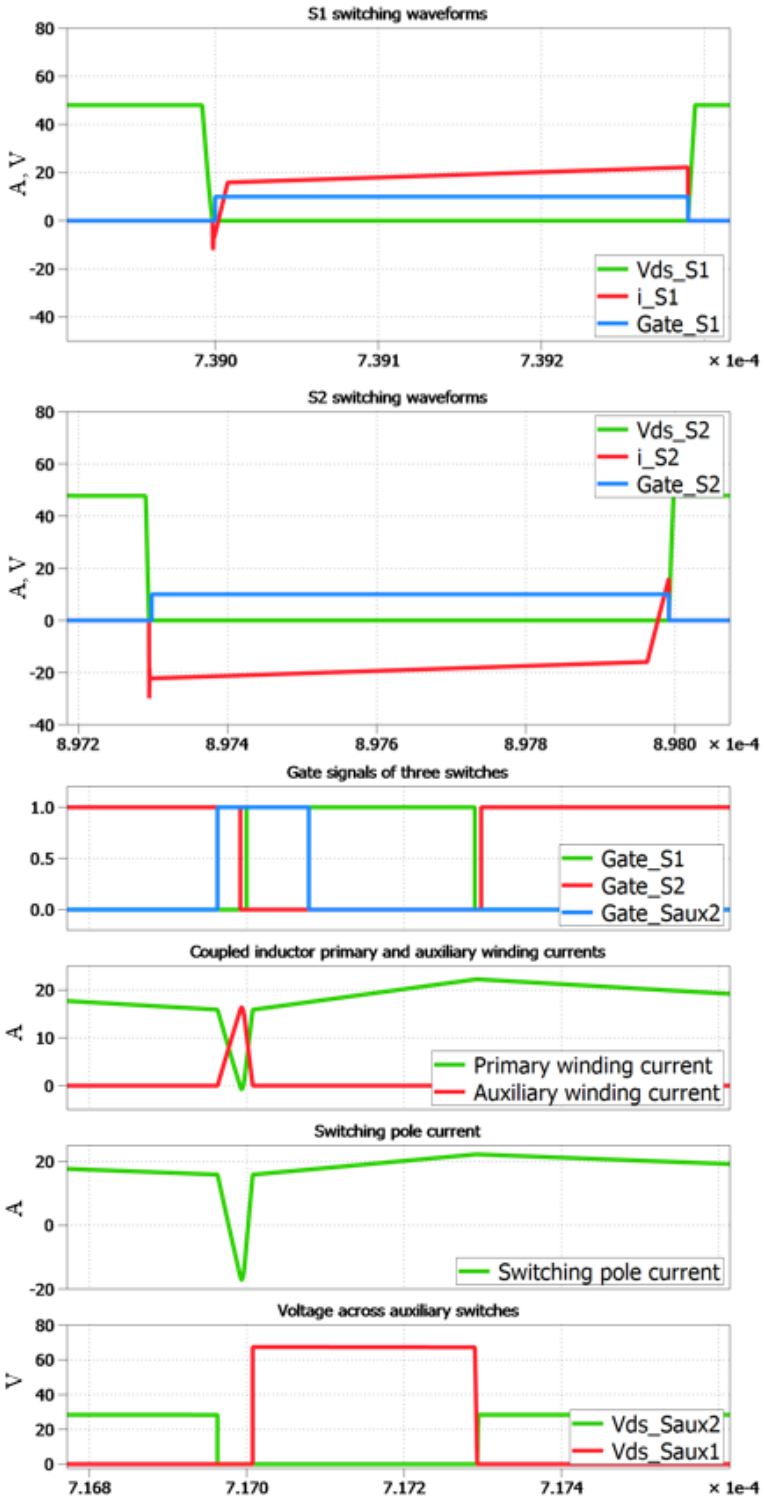


Figure 3.12: Simulation Results under Buck Mode Operation.

Table 3.2: Designed Parameters

Coupled-Inductor Turns Ratio $1:n$	1 : 1
Magnetizing Inductance L_m	1.5 uH
Leakage Inductance L_l	40 nH
Output Capacitance C_o	80 uF
Resonant Capacitance C_r	1.2 nF

3.6 Experimental Verification

3.6.1 Hardware Implementation

Design of the Coupled-Inductor

A converter prototype per the specifications shown in Table 3.1 is built to verify the operation of the proposed converter. The coupled-inductor is a key component in this prototype. For this design, the required leakage inductance is 40 nH while the magnetizing inductance is 1.5 uH. This requires a high coupling coefficient of 0.973. For the conventional design with vertical cores and wire-based windings, it is difficulty to achieve such a high coupling coefficient. Moreover, it is hard to precisely control the leakage inductance to the designed value. In this prototype, a planar core structure and PCB windings are employed for the coupled-inductor because they can provide low and controllable leakage inductance. Furthermore, the fabrication of planar design with PCB windings makes it easier to achieve repeatable and significantly lower parameter tolerance between two coupled-inductors, which is critical for a multiphase converter considering the current sharing issue [59, 60].

Figure 3.13 shows 2D structure of the designed coupled-inductor. Two separate

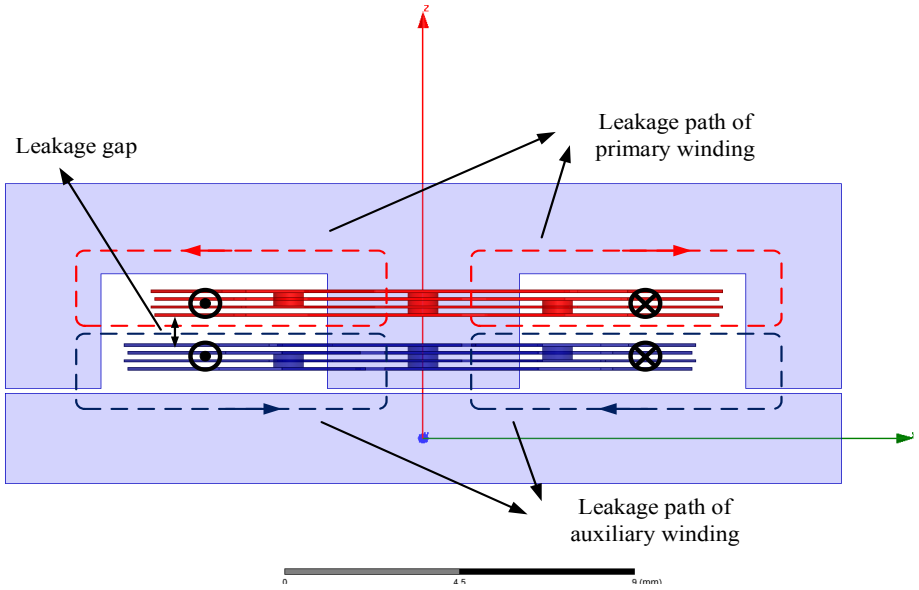


Figure 3.13: 2D Structure of the Designed Coupled-inductor.

but same 4-layer PCBs are employed as primary and auxiliary windings, respectively. It is clearly shown that part of the leakage path is the gap between two PCB windings. Therefore, by adjusting this gap distance and hence the leakage path reluctance, the leakage inductance of the coupled-inductor could be controlled to a small value. Figure 3.14 is Maxwell 3D model of the designed coupled-inductor. Finite-element-analysis simulation is employed to calculate the gap between two PCBs. Table 3.3 shows the designed parameters for this coupled-inductor. A ferrite core 3F45 from Ferroxcube suitable for <3MHz operation is chosen. For each PCB, each layer has only one turn and the configuration is paralleled layer 1 and 3, in series with paralleled layer 2 and 4. For further improving the efficiency, two 6-layer PCBs could be employed to reduce DCR.

The constructed coupled-inductor is shown in Figure 3.15. The measured leakage inductance is 30 nH. Considering the PCB trace and interconnection stray inductance, the total leakage inductance is around 35 - 40 nH, as desired. In fact, once the

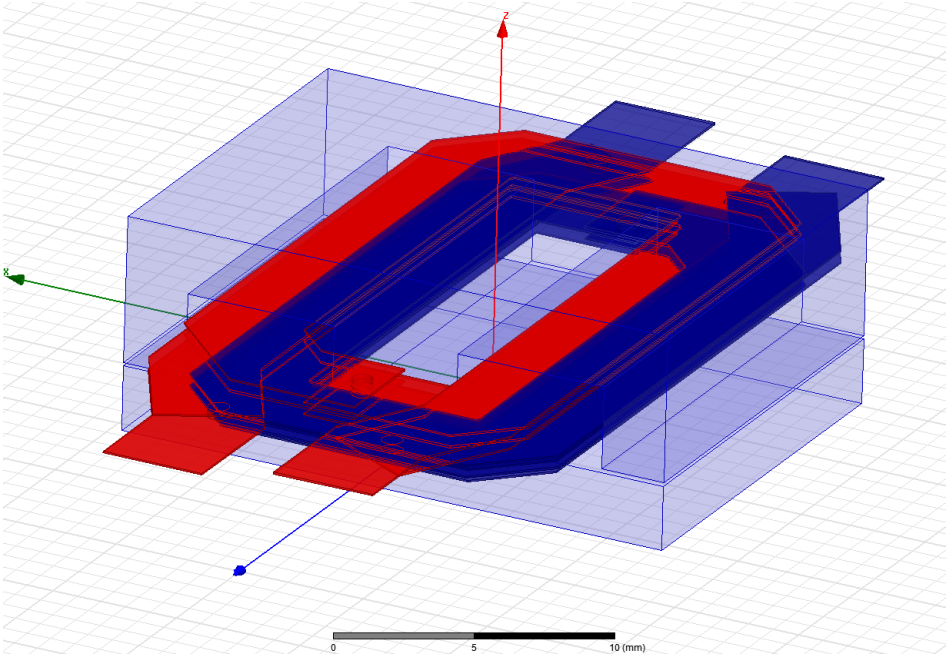


Figure 3.14: 3D Structure of the Designed Coupled-inductor.

Table 3.3: Designed Parameters of the Coupled Inductor

Core Material	3F45
Core Shape	E22/6/16+PLT22/16/2.5
Primary/Auxiliary Number of Turns	2 turns
ΔB_{max}	60 mT
DCR	3.1 mΩ
Air Gap l_g	0.3 mm
Leakage Gap	0.2 mm

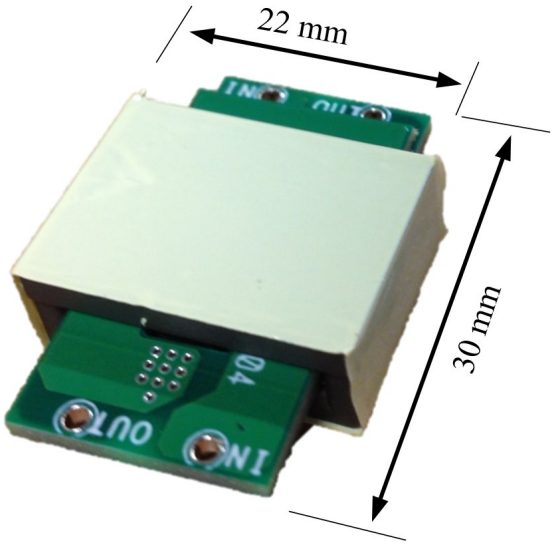


Figure 3.15: Constructed Coupled-inductor.

leakage gap is finalized by experiment, only one PCB is enough for both primary and secondary windings, with distance between two winding layers the same as the leakage gap. Since the secondary winding carries very small average current, only one layer is enough for the secondary winding. Then, the secondary winding almost takes no space, and the coupled-inductor size could be kept the same as the filter inductor size in conventional buck converter.

Power Stage Design

The built 1 MHz, 250 W prototype is shown in Figure 3.16. The schematic and layout design for this prototype are given in Appendix B. Table 3.4 shows the key components selection and parameters.

3.6.2 Experimental Results

Figure 3.17 shows the gate signals of S_1, S_2 and S_{aux2} in buck mode operation. S_{au1} is kept off in buck mode. Figure 3.18 and 3.19 are the switching waveforms of S_1 and S_2, respectively, at 48 V input, 14 V output and 15 A load. It could be seen that

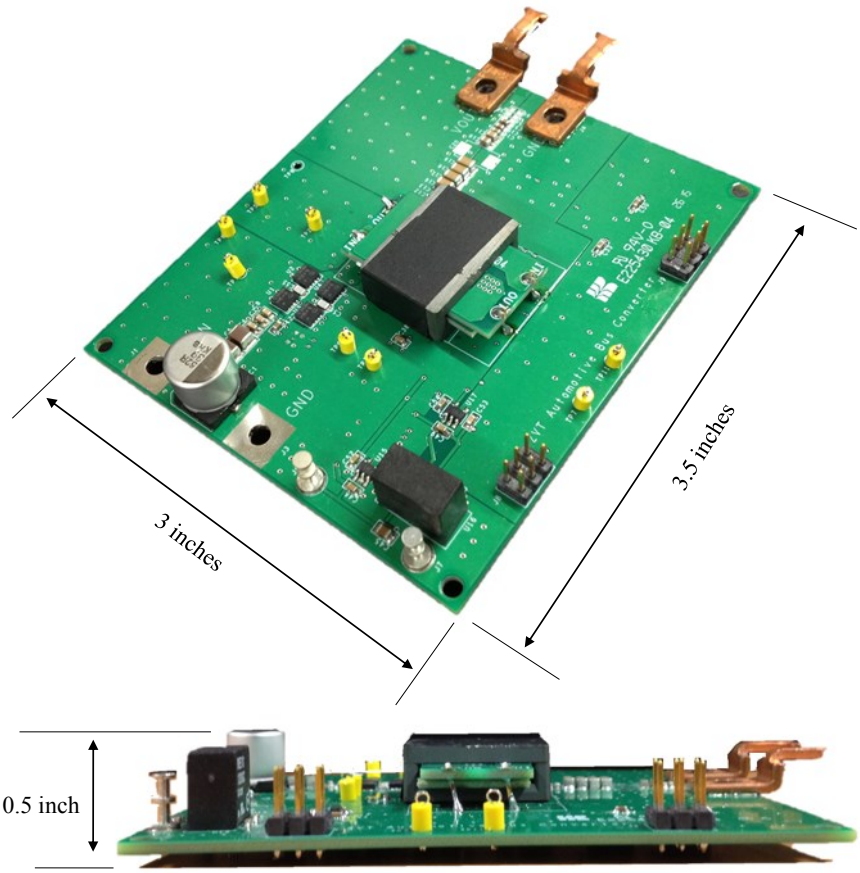


Figure 3.16: 1 MHz, 250 W Prototype of the Proposed Bidirectional ZVT Converter with Coupled-inductor.

Table 3.4: Key Components Selection and Values

Components	Part Number	Parameters
Main MOSFETs	BSZ123N08NS3G	80V, 12.3mΩ, 6.3nC
Auxiliary MOSFETs	BSZ440N10NS3G	100V, 44mΩ, 9.1nC
Main MOSFETs driver	UCC27211	bootstrap
Auxiliary MOSFETs driver	UCC27524	2-channel, low side

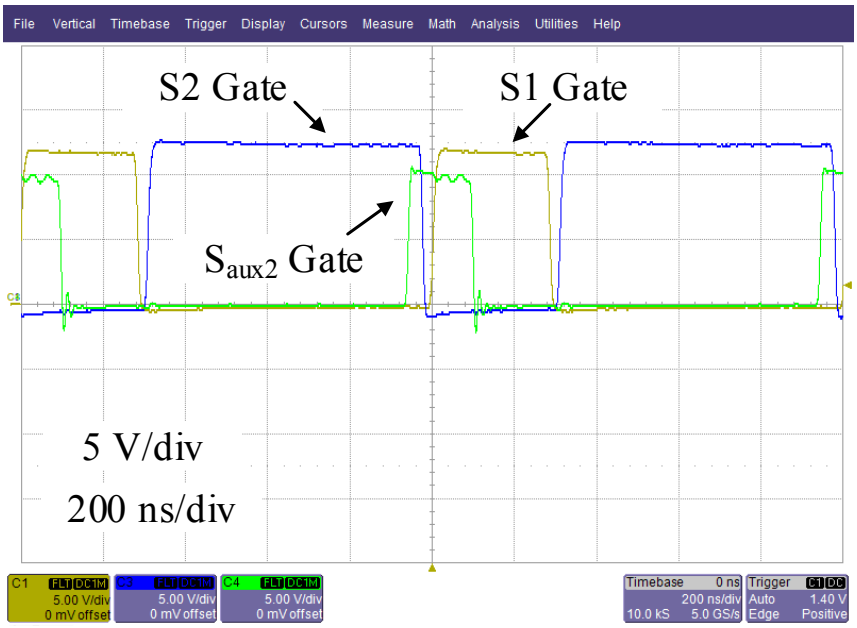


Figure 3.17: Gate Signals in Buck Mode.

ZVS of both switches are realized. At light load, ZVS realization of S_1 is more easily. In addition, since two small capacitors are paralleled with S_1 and S_2, respectively, slowing the voltage rising during turn-off transition, the turn-off of S_1 and S_2 is almost ZVS. Figure 3.20 shows the voltage waveforms across auxiliary MOSFETs in buck mode operation. The waveforms present some ringings. The voltage ringing in S_{aux1} waveform is due to the resonance between the leakage inductance and C_{oss} of S_{aux1} when the body-diode of S_{aux1} turns off. The ringing on S_{aux2} waveform happens when the load current transfers from S_1 to S_2 (body-diode). It is resulted from the resonance between the leakage inductance and C_{oss} of S_{aux2}.

The waveforms associated with boost mode operation are also shown. Figure 3.21 is the gate signals of S_1, S_2 and S_{aux1}, and S_{aux2} is constantly off in boost mode. The switching waveforms of S_1 and S_2, at 14 V input, 48 V output and 4 A load, are shown in Figure 3.22 and 3.23, respectively. Both switches can achieve ZVS turn-on and almost ZVS turn-off. Figure 3.24 shows the auxiliary MOSFETs voltage

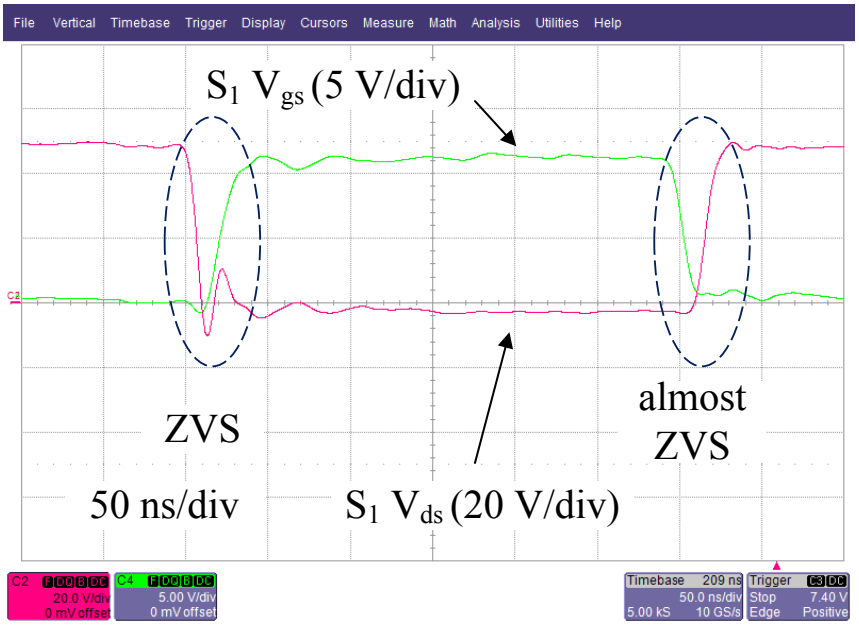


Figure 3.18: Switching Waveforms of S_1 in Buck Mode.

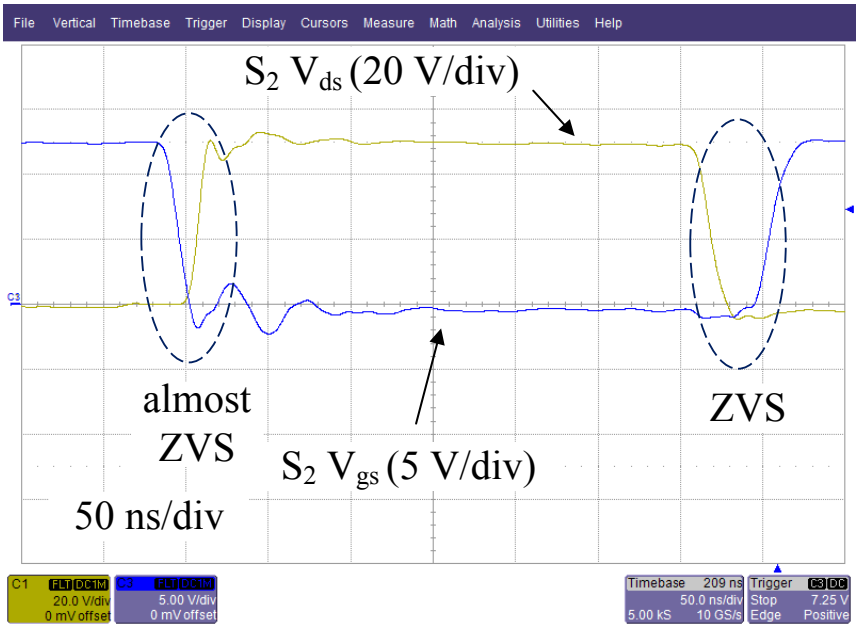


Figure 3.19: Switching Waveforms of S_2 in Buck Mode.

Figure 3.20: Voltage Waveforms of Auxiliary MOSFETs in Buck Mode.

waveforms. Still, S_{aux1} withstands the higher voltage at steady state.

The conversion efficiency of this prototype is also measured for both buck mode (48 V to 14 V) and boost mode (14 V to 48 V) operations. The efficiency curves at different output power are shown in Figure 3.25 and 3.26. A peak efficiency of 93.98% is achieved in buck mode operation. In boost mode operation, the peak efficiency achieved is 92.99%. For comparison, the measured efficiency data from a hard-switching buck/boost converter with the same circuit parameters and components is shown in Figure 3.25 and 3.26 as well. It could be seen that the proposed ZVT converter with coupled-inductor has significantly improved efficiency performance.

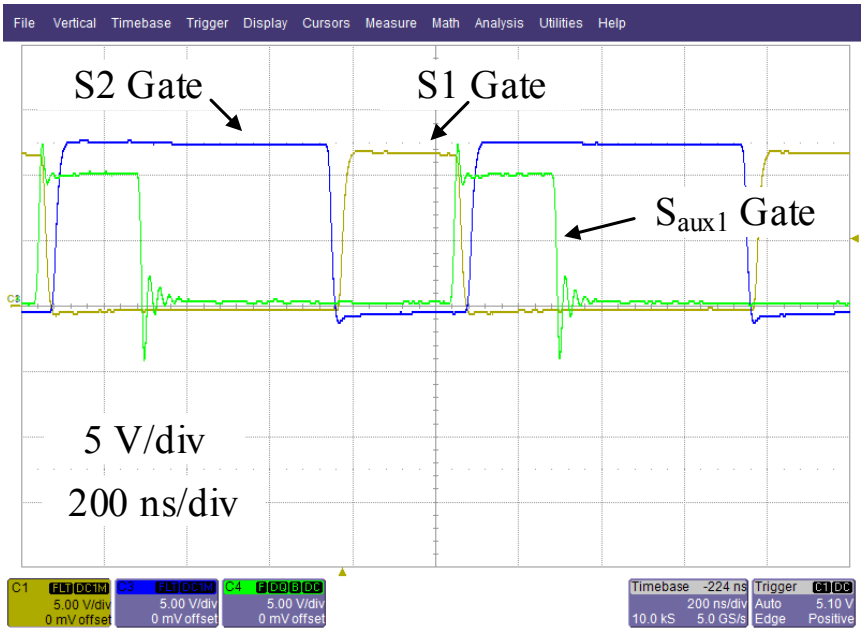


Figure 3.21: Gate Signals in Boost Mode.

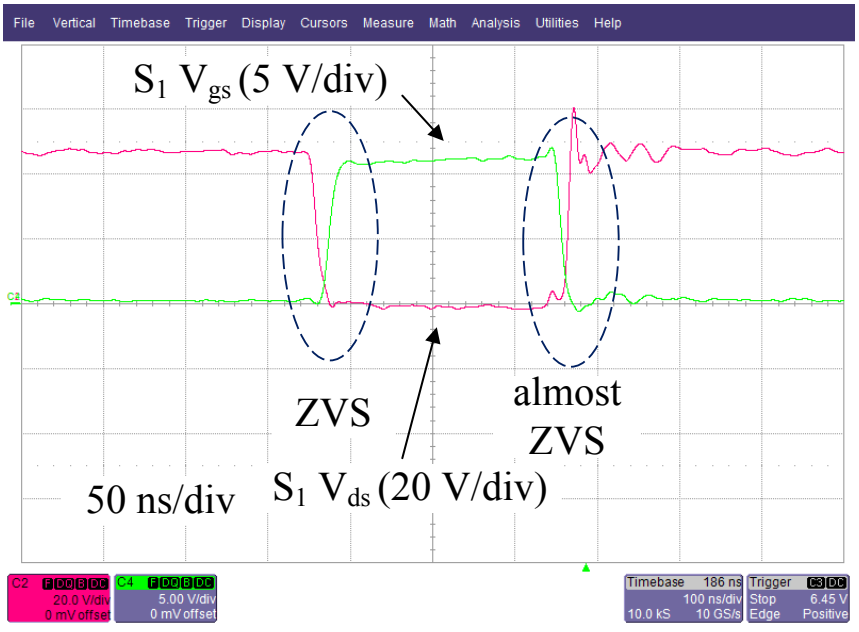


Figure 3.22: Switching Waveforms of S_1 in Boost Mode.

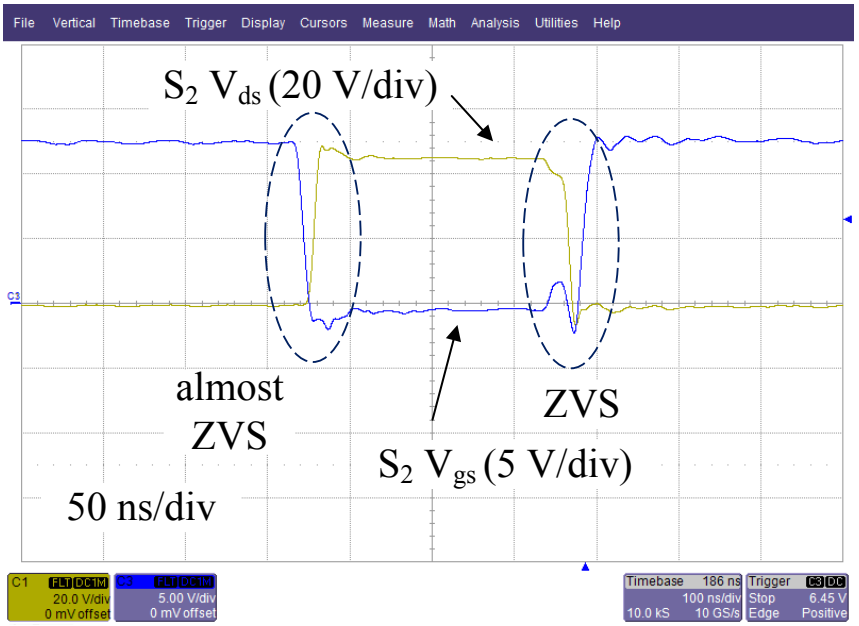


Figure 3.23: Switching Waveforms of S_2 in Boost Mode.

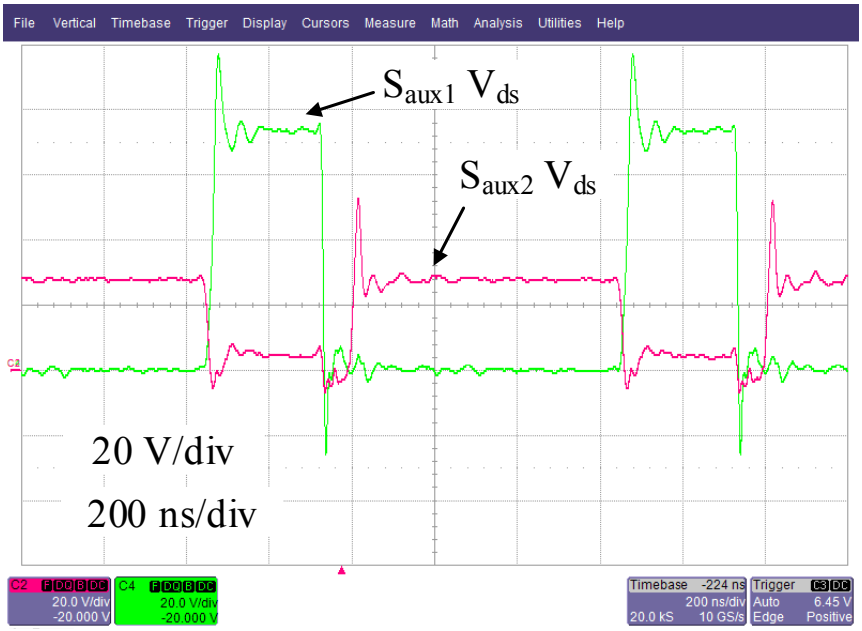


Figure 3.24: Voltage Waveforms of Auxiliary MOSFETs in Boost Mode.

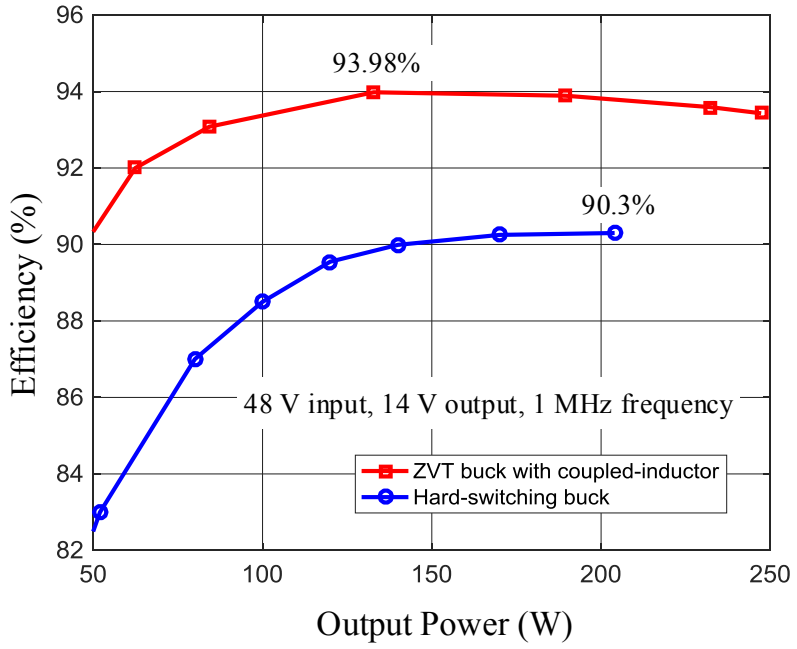


Figure 3.25: Efficiency Comparison in Buck Mode.

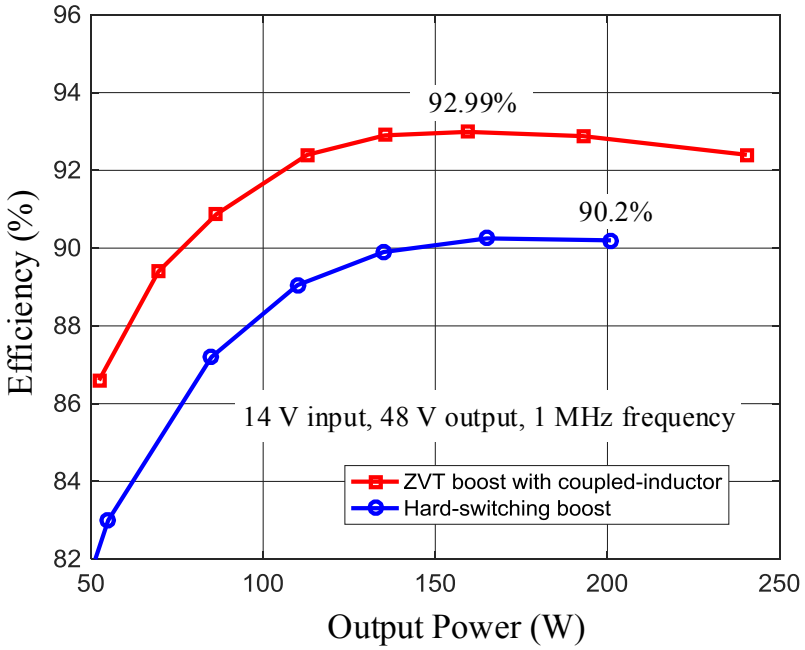


Figure 3.26: Efficiency Comparison in Boost Mode.

3.7 Summary

In this chapter, a novel bidirectional ZVT converter with coupled-inductor is proposed for automotive dual voltage system. With the combination of the ZVT circuit and coupled-inductor, this converter requires less current in the auxiliary cell to realize ZVS operation of main MOSFETs. Generally, this converter features high efficiency, low EMI noise, scalability for high power output, and low profile design. The detailed operating principle analysis of the proposed converter is presented. Several important design considerations, including ZVS analysis, auxiliary switch gate timing, leakage inductance design and selection of the coupled-inductor turns ratio, are also presented. A 1 MHz, 250 W prototype converter with planar magnetic structure is then built and tested. The comprehensive experimental results verify the converter operation in both buck and boost mode. The measured efficiency data shows peak efficiencies of 93.98% in buck mode and 92.99% in boost mode are achieved. Moreover, the efficiency comparison indicates the proposed ZVT converter with coupled-inductor has significant efficiency improvement than hard-switching bidirectional buck/boost converter.

Chapter 4

CONCLUSION AND FUTURE WORK

4.1 Conclusion

In this thesis work, the electrical systems in automobiles, including the present 14-V PowerNet architecture and future 48V/14V dual voltage architecture, are firstly introduced. Then, the system requirements for automotive dc-dc converters are studied. The major design challenging includes the wide voltage range at the converter input and the requirement of low EMI noise operation. The hard-switching (synchronous) buck converter is firstly reviewed. Although it is currently widely used in industry, buck converter has several drawbacks: 1) hard-switching and hence low efficiency at high switching frequency; 2) high EMI noise emission due to the hard-switching. Thus, the buck converter is not perfect for automotive applications. Then, various known soft-switching topologies are reviewed. However, each of them suffers from one or more issues for the given automotive applications. Therefore, in this thesis, two novel soft-switching topologies are proposed.

First, a new active-clamp buck topology is proposed for automotive POL converters. Comprehensive analysis for this topology is given. Then a 2.2MHz, 5V/5A active-clamp buck converter is designed and constructed. The experimental results verify the converter operation and the efficiency measurement shows 89.7% peak efficiency with 12V/5V conversion. Detailed loss breakdown is presented. In order to further improve the efficiency, GaN FET as well as optimal SR turn-off delay are employed. The peak efficiency is then improved to 93.22%. In addition, the EMI test results show that the proposed active-clamp buck converter has significantly better

EMI performance than hard-switching buck converter. Last, the modeling of the proposed active-clamp buck converter is addressed. The large-signal averaged model and small-signal model are derived and verified with simulation, respectively. It shows that the response in the derived models matches very well to the response in the simulation with switching circuit model.

Then, for the automotive 48V/14V dual voltage system, a new bidirectional ZVT converter with coupled-inductor is proposed. This converter features high efficiency and low noise operation. In addition, it is flexible for interleaving and the size of the converter could be very compact. The detailed operating principle of this converter and several design considerations are presented. A 1 MHz, 250 W prototype converter with planar coupled-inductor is then built and tested. The comprehensive experimental results verify the operation of the converter in both buck and boost mode. The peak efficiencies are measured at 93.98% in buck mode and 92.99% in boost mode. Moreover, significant efficiency improvement is achieved from the efficiency comparison between the proposed converter and hard-switching buck converter.

4.2 Suggestions for Future Work

In automotive applications, high switching frequency of dc-dc converters is desired to avoid AM band and reduce the converter size. In this thesis, soft-switching topologies are employed to achieve better efficiency at high switching frequency. There is also another way to achieve compact size and possible better efficiency by employing multilevel converters or emerging switched capacitor based hybrid converters. By using more active switches, the passive components in these converters could be much reduced at a moderate switching frequency. However, in most of these converters, hard-switching still exists and affects the efficiency. Some resonant switched capacitor converters can achieve ZVS or ZCS but regulation capability is lost. Therefore, it

is worth to investigate more on multilevel converters and switched capacitor based hybrid converters, and see if it is possible to combine both soft-switching and regulation capability on these converters.

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APPENDIX A

SCHEMATIC AND LAYOUT DESIGN FOR 2.2MHZ, 5V/5A ACTIVE-CLAMP BUCK WITH SI MOSFETS

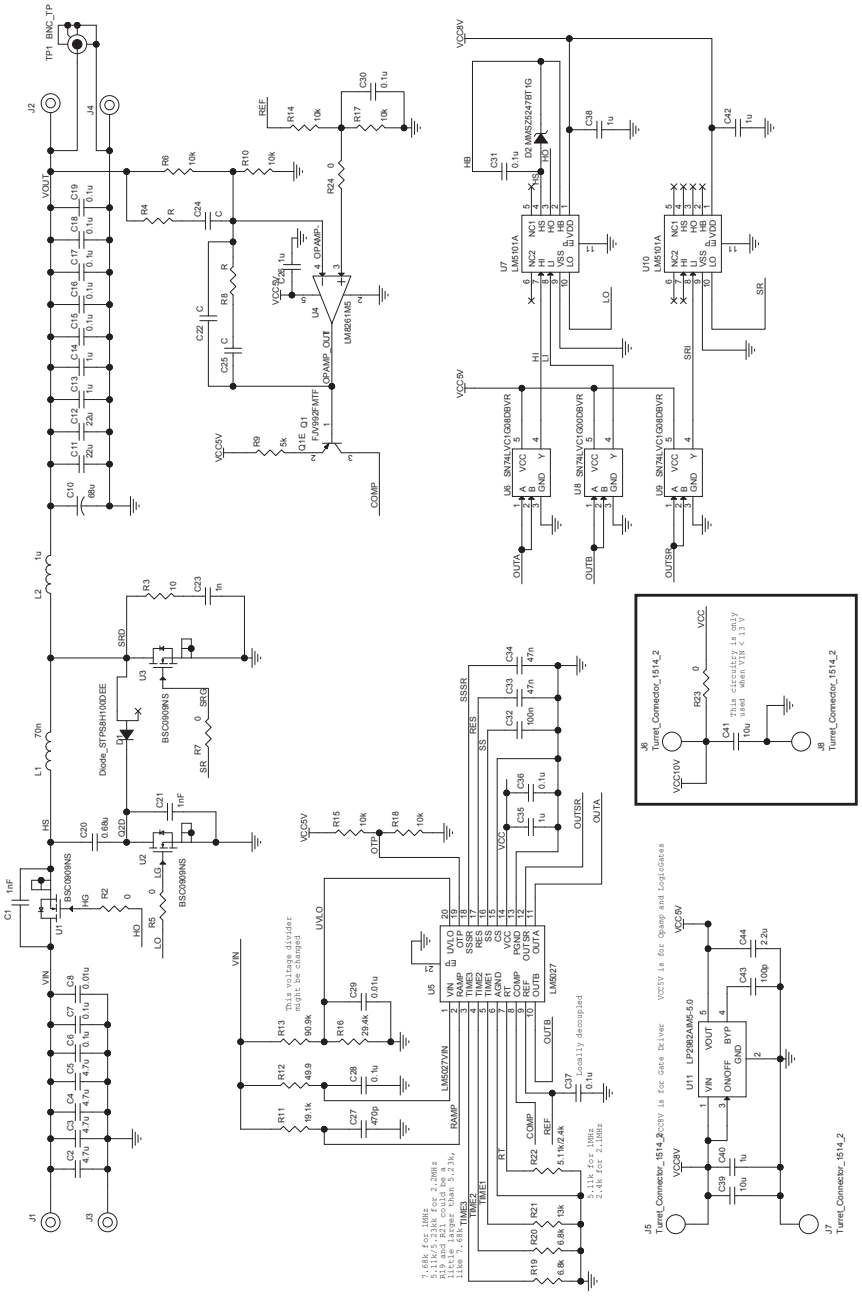

Figure A.1: Schematic Design.

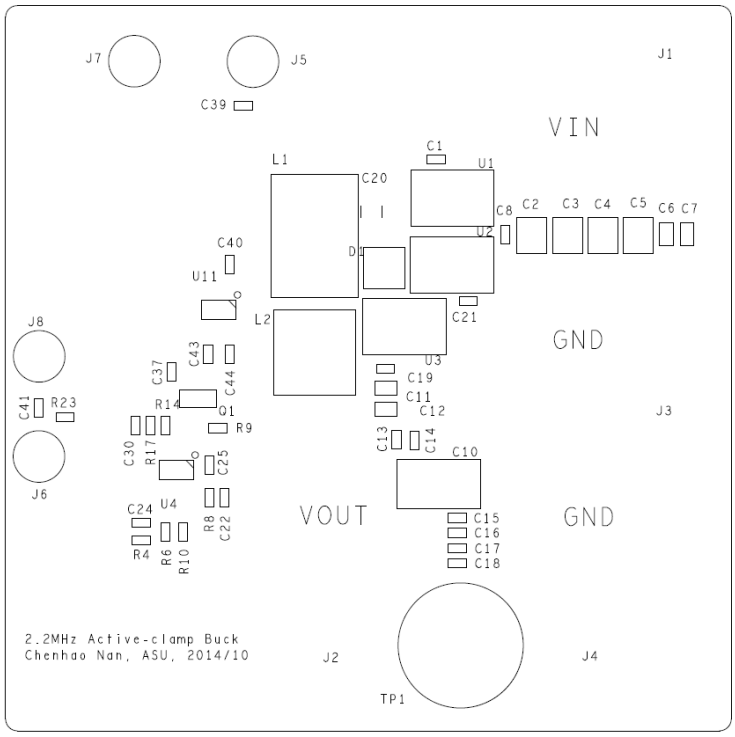

Figure A.2: Top Layer Silkscreen.

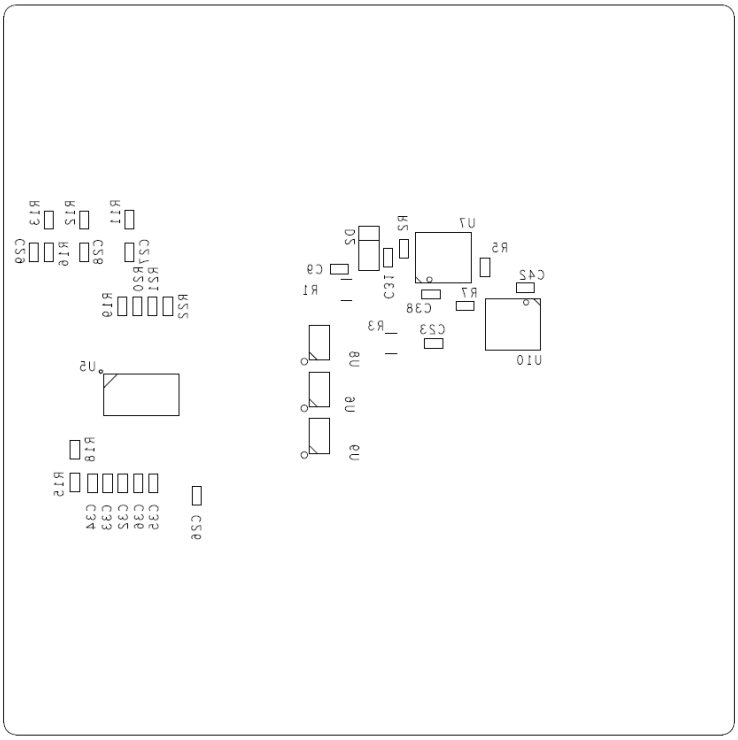

Figure A.3: Bottom Layer Silkscreen.

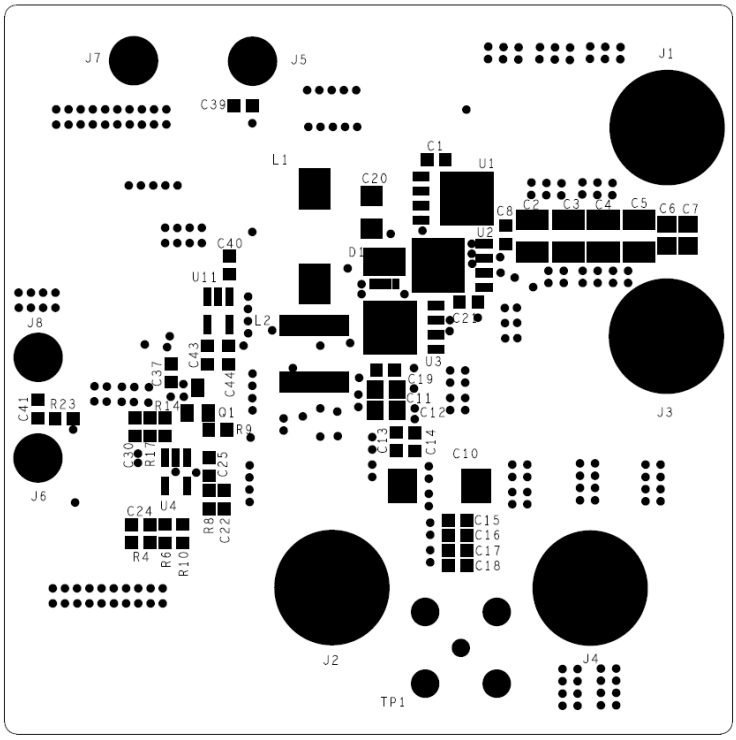

Figure A.4: Top Layer Soldermask.

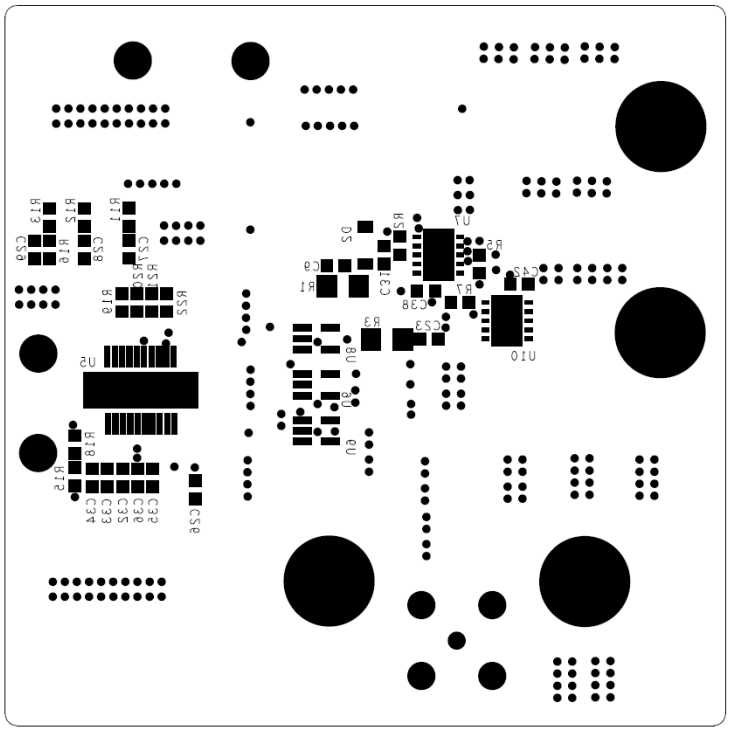

Figure A.5: Bottom Layer Soldermask.

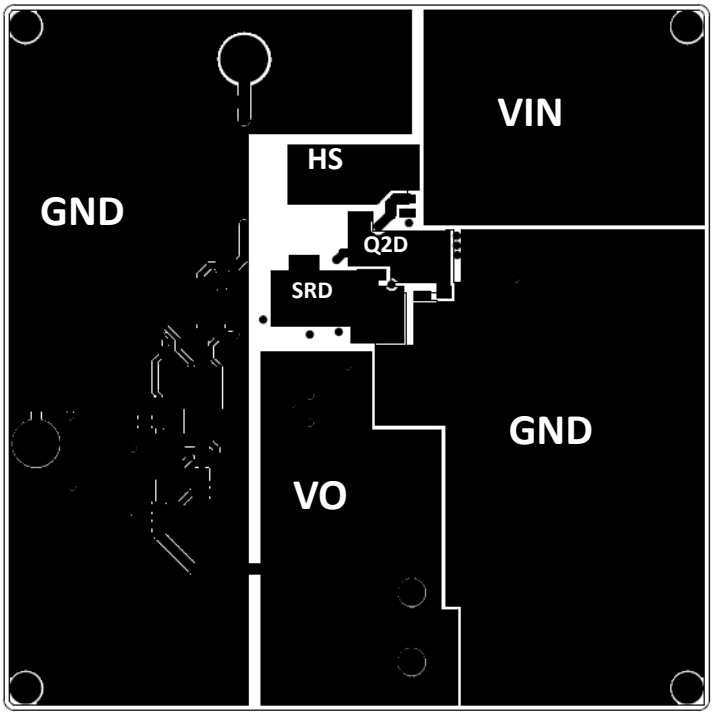

Figure A.6: Top Layer Copper.

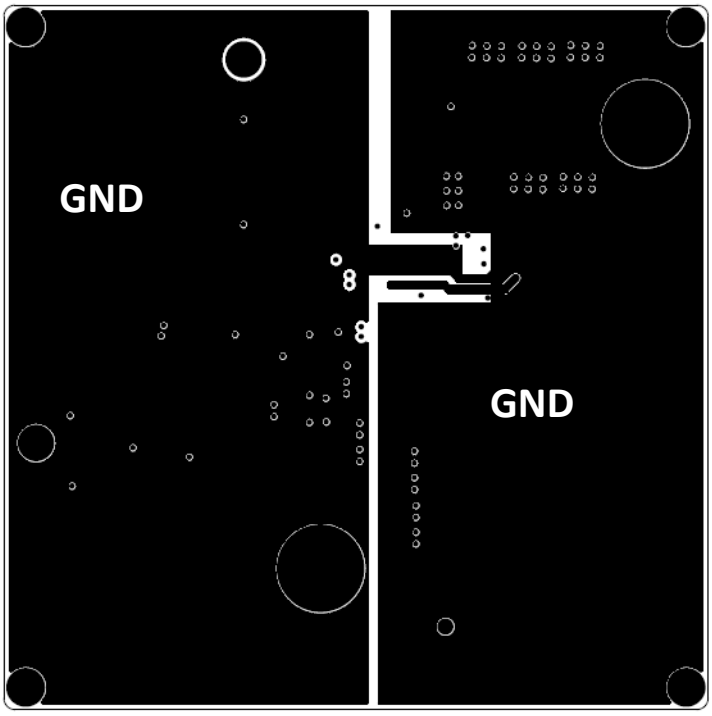

Figure A.7: Second Layer Copper.

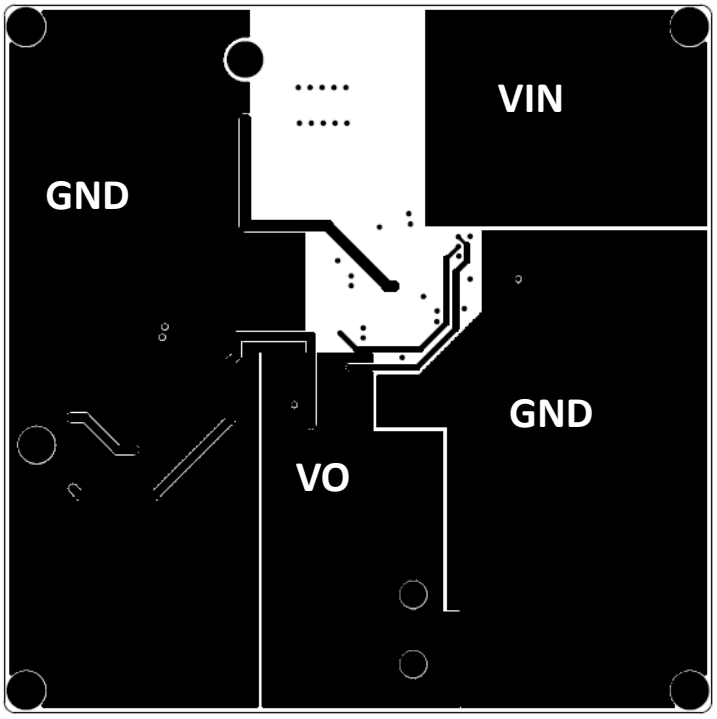

Figure A.8: Third Layer Copper.

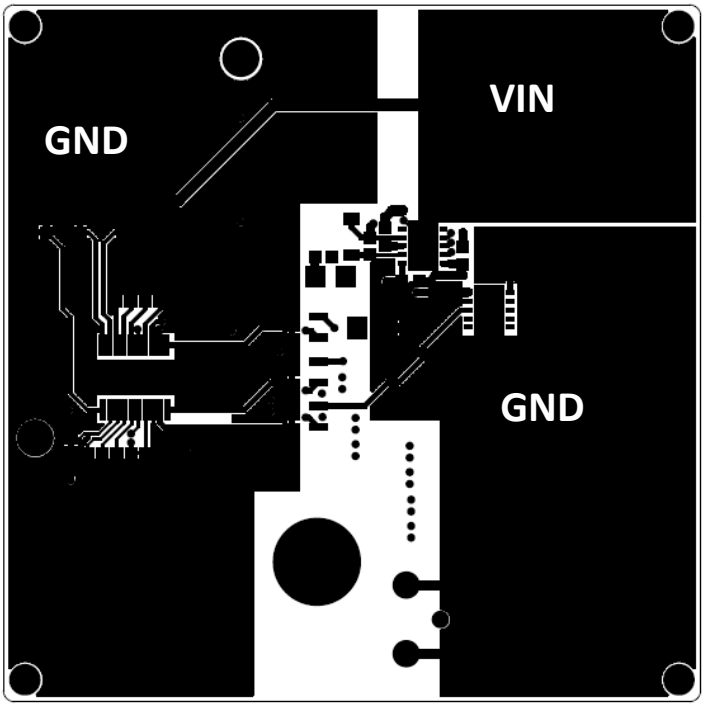

Figure A.9: Bottom Layer Copper.

APPENDIX B

SCHEMATIC AND LAYOUT DESIGN FOR 2.2MHZ, 5V/5A ACTIVE-CLAMP BUCK WITH GAN FETS

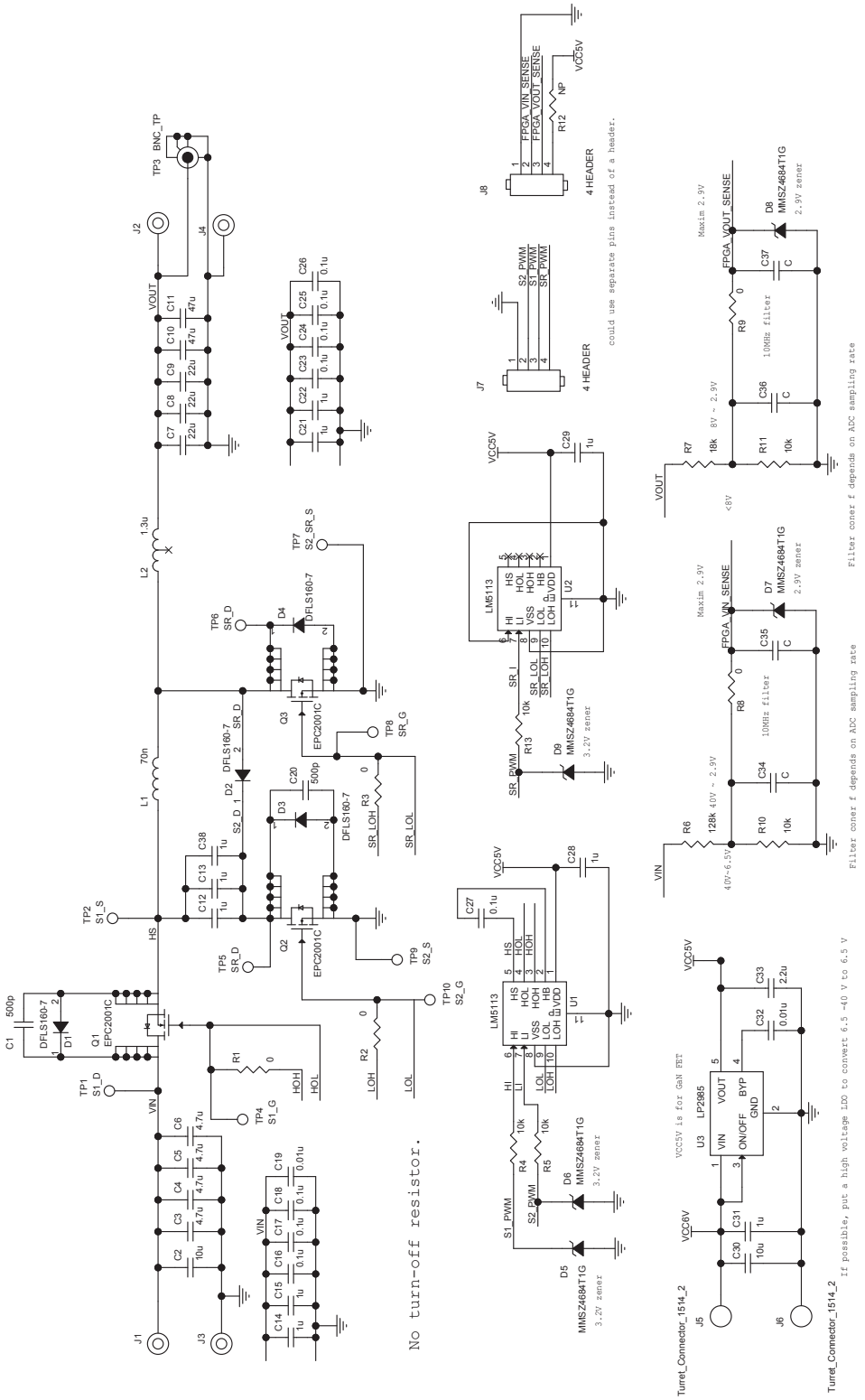

Figure B.1: Schematic Design with GaN Devices.

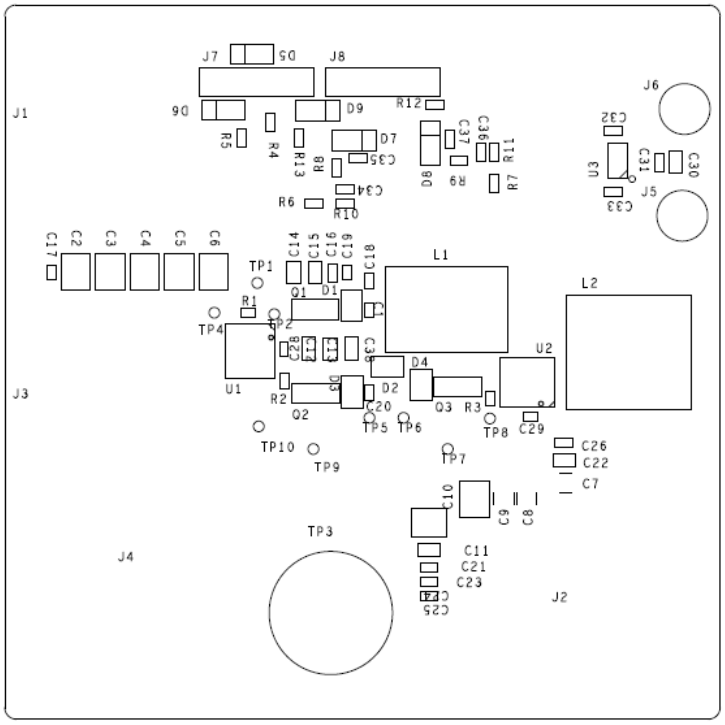

Figure B.2: Top Layer Silkscreen.

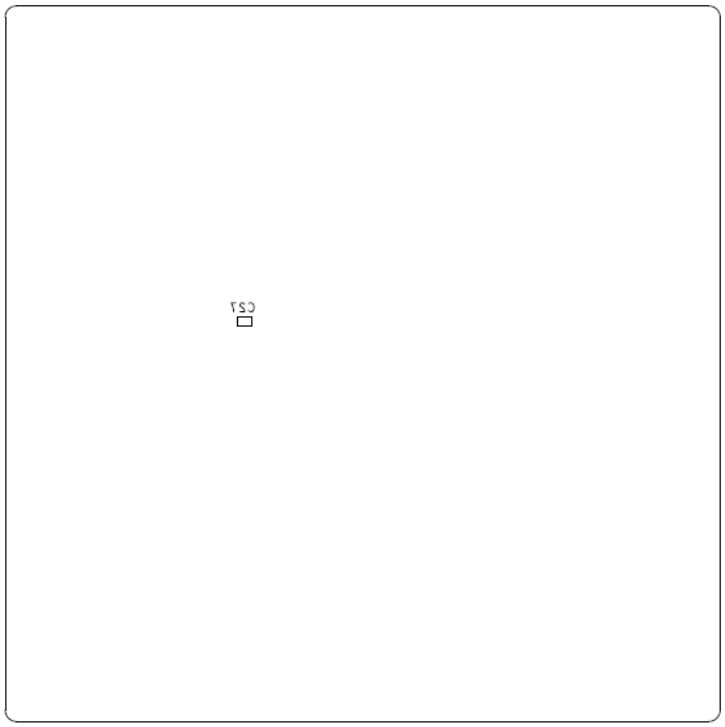

Figure B.3: Bottom Layer Silkscreen.

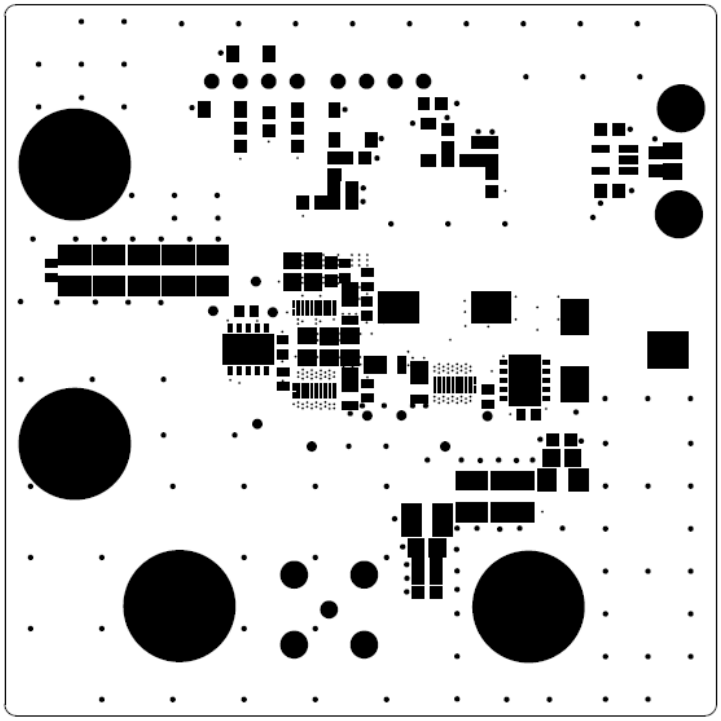

Figure B.4: Top Layer Soldermask.

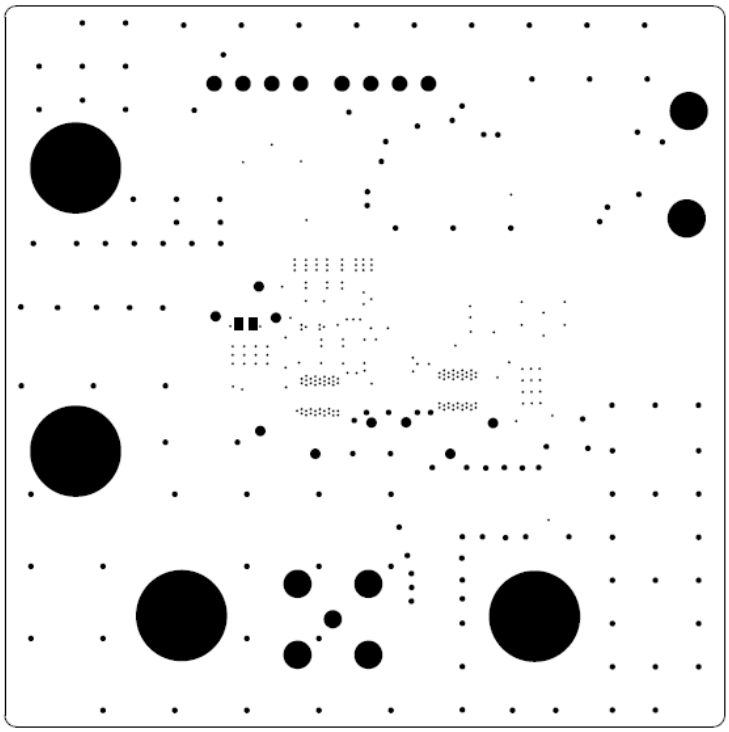

Figure B.5: Bottom Layer Soldermask.

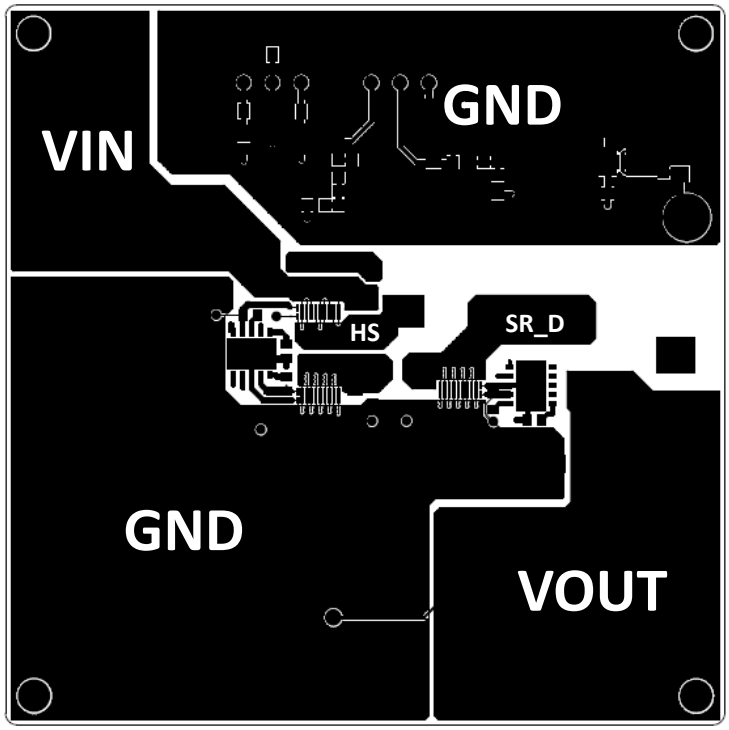

Figure B.6: Top Layer Copper.

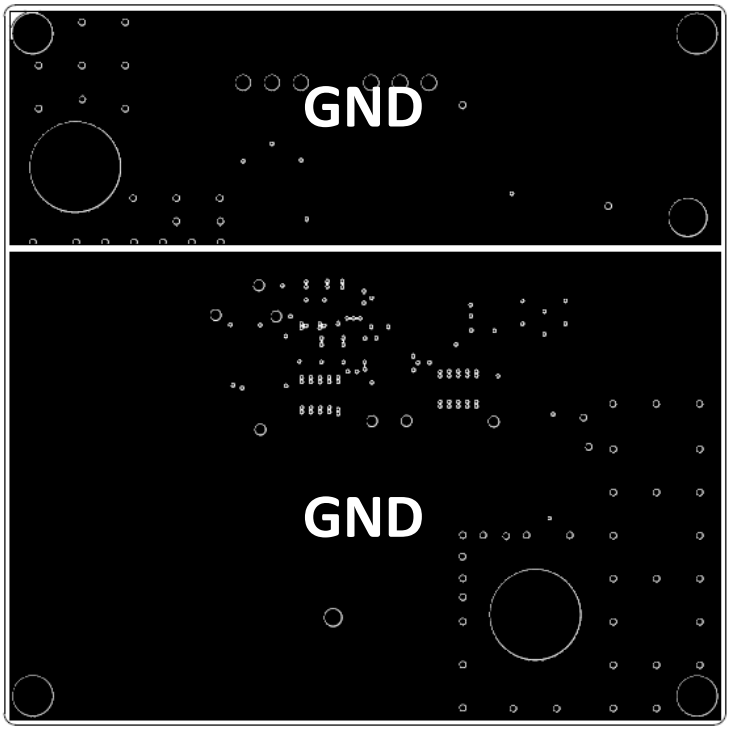

Figure B.7: Second Layer Copper.

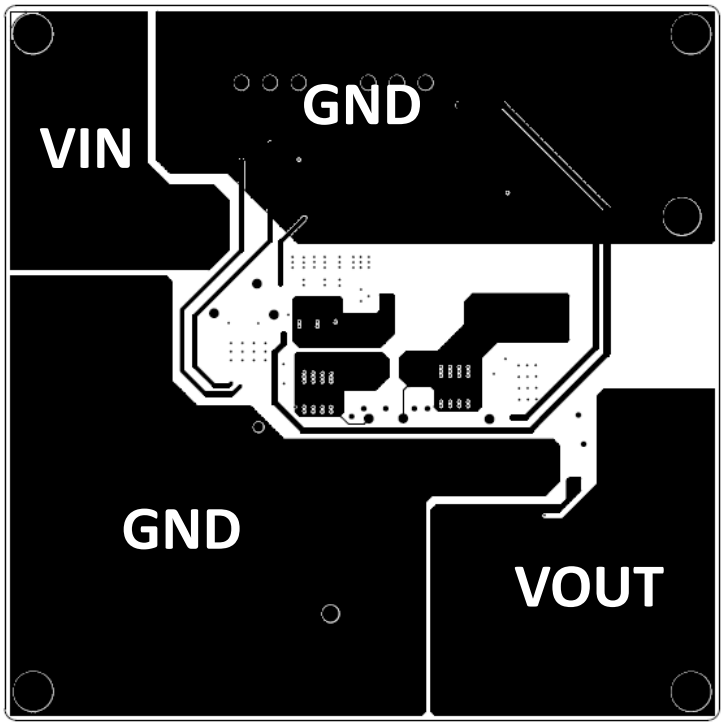

Figure B.8: Third Layer Copper.

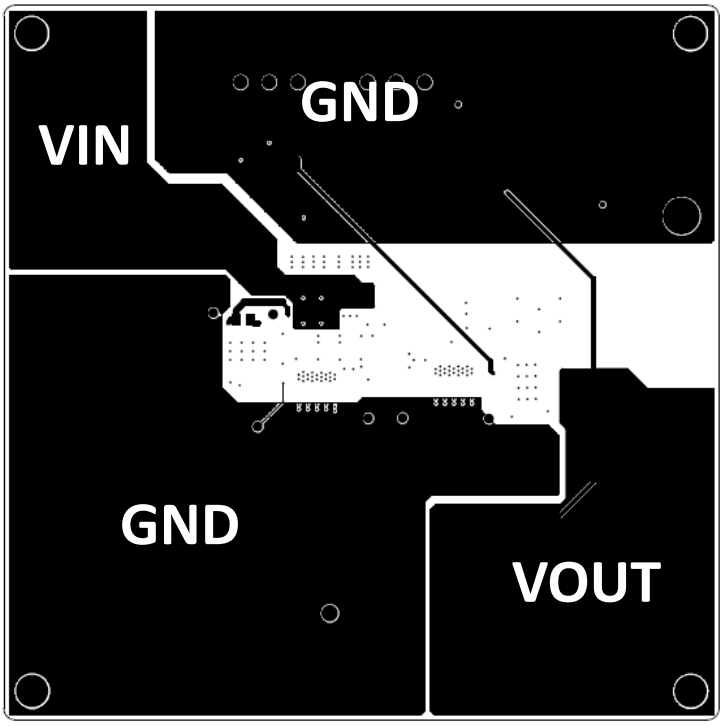

Figure B.9: Bottom Layer Copper.

APPENDIX C

SCHEMATIC AND LAYOUT DESIGN FOR 1 MHZ, 48V/14V, 250 W ZVT BIDIRECTIONAL CONVERTER WITH COUPLED-INDUCTOR

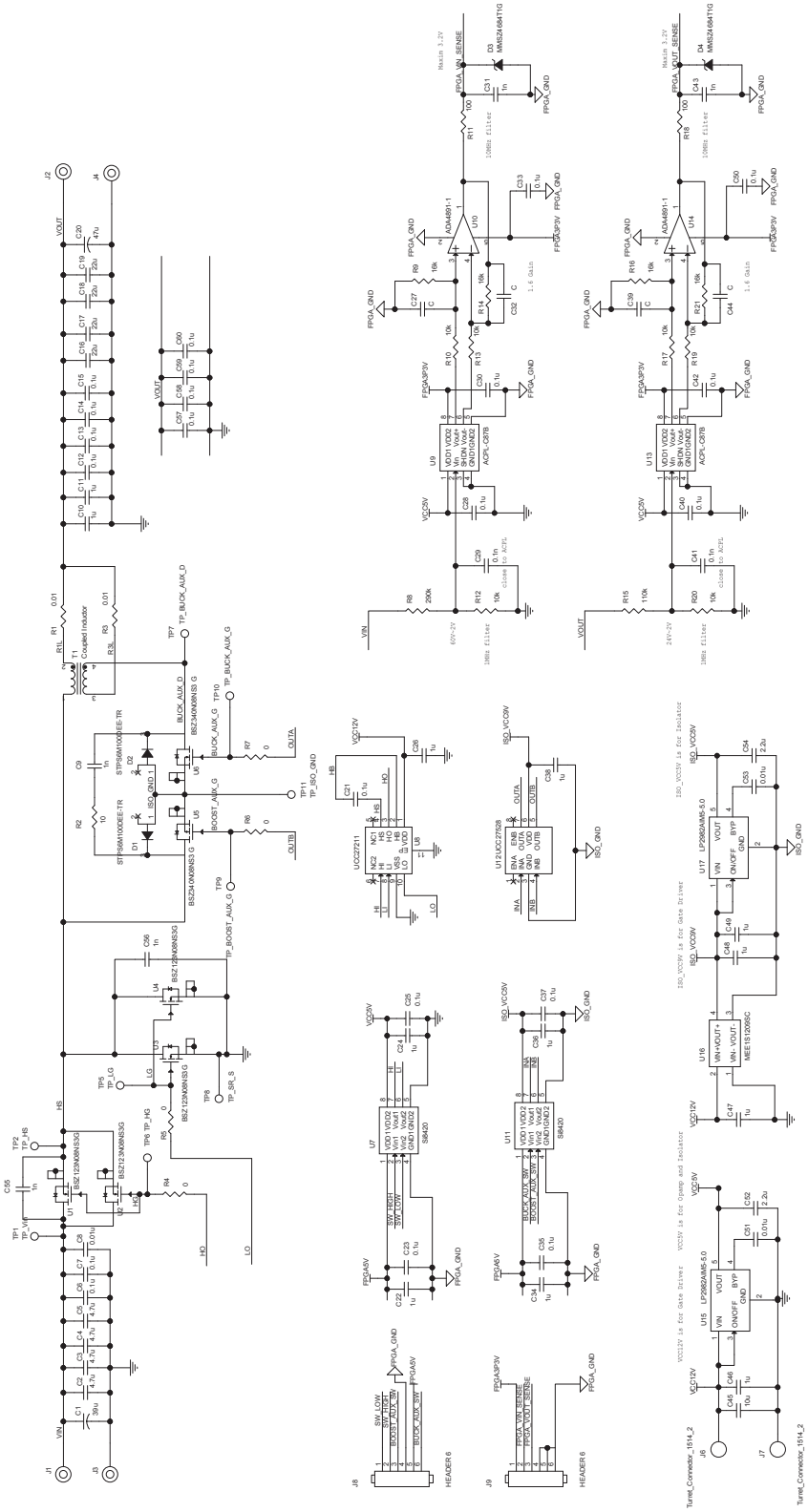

Figure C.1: Schematic Design.

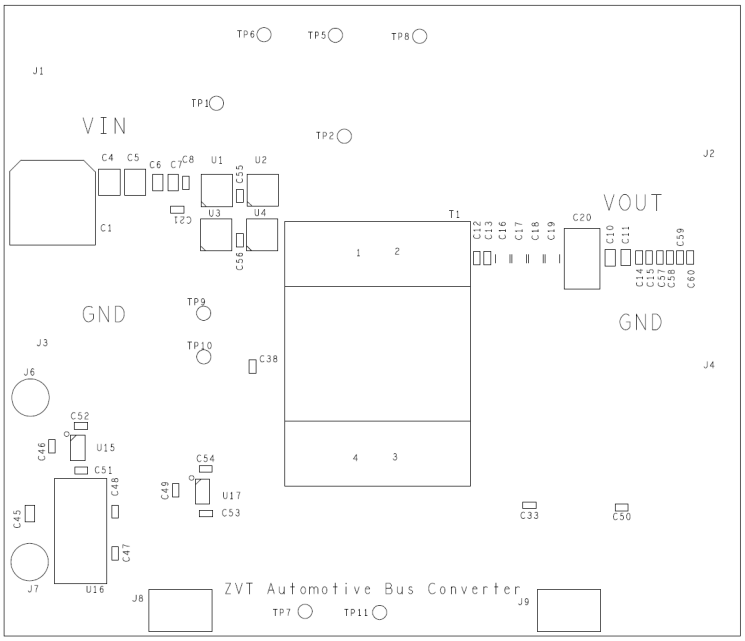

Figure C.2: Top Layer Silkscreen.

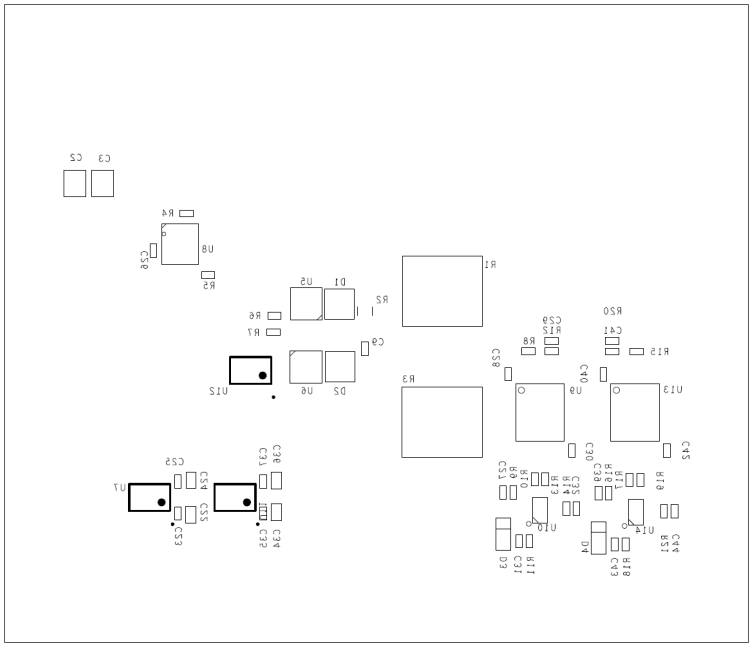

Figure C.3: Bottom Layer Silkscreen.

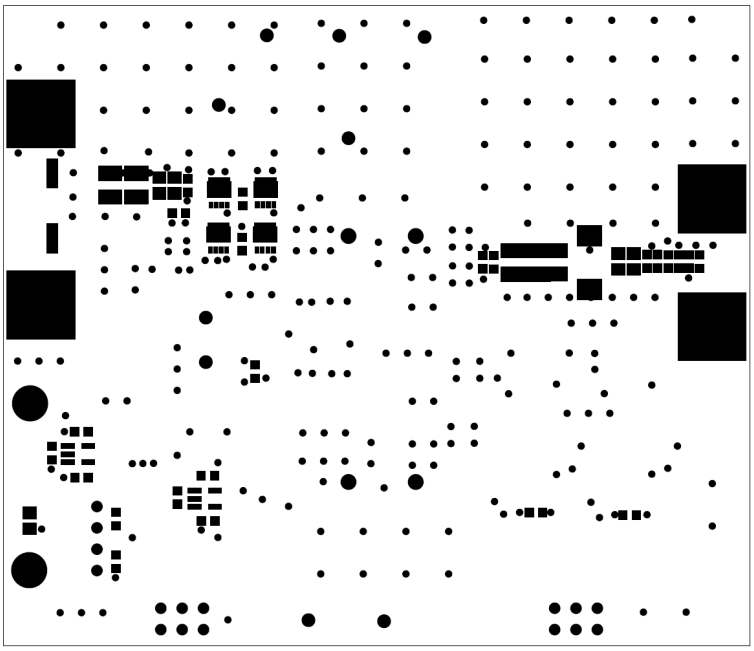

Figure C.4: Top Layer Soldermask.

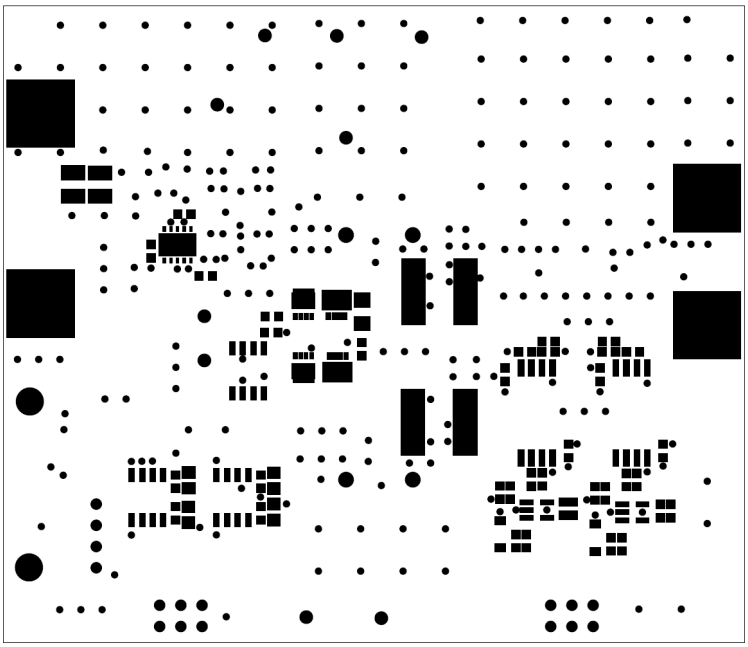

Figure C.5: Bottom Layer Soldermask.

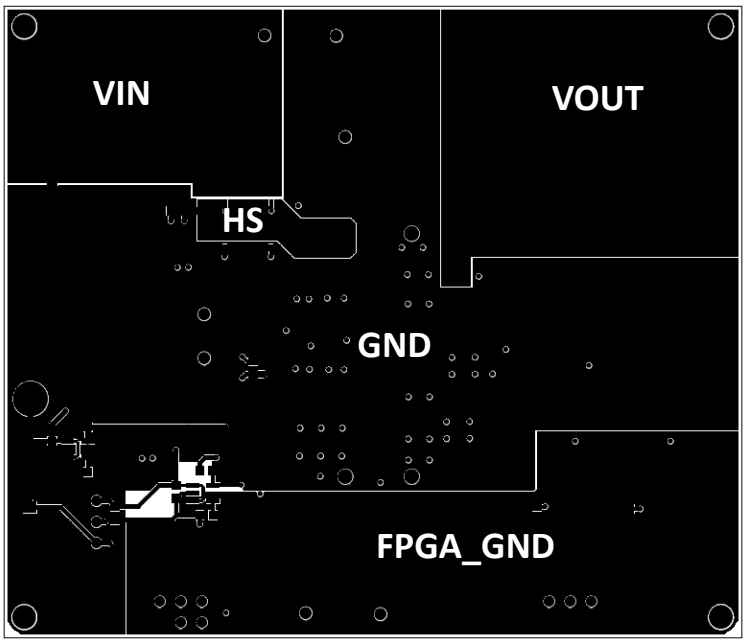

Figure C.6: Top Layer Copper.

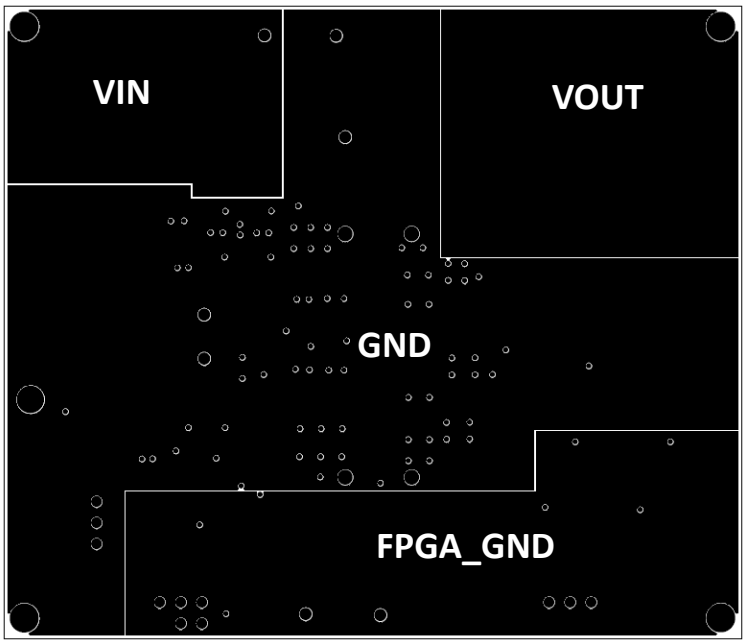

Figure C.7: Second Layer Copper.

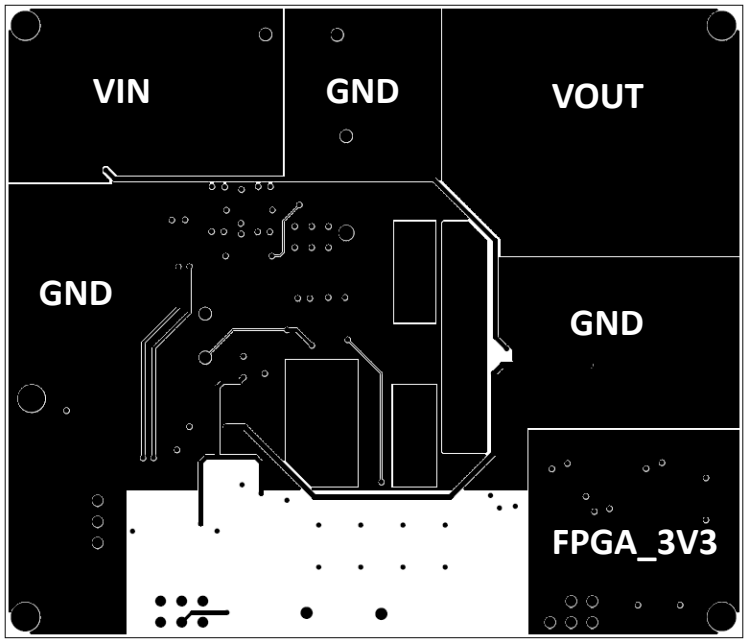

Figure C.8: Third Layer Copper.

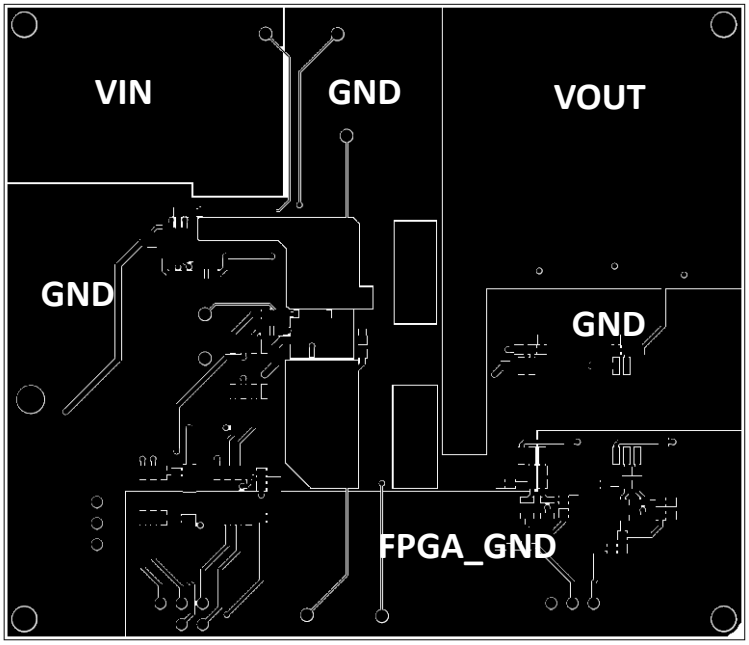

Figure C.9: Bottom Layer Copper.